3D IC Packaging and 3D IC Integration

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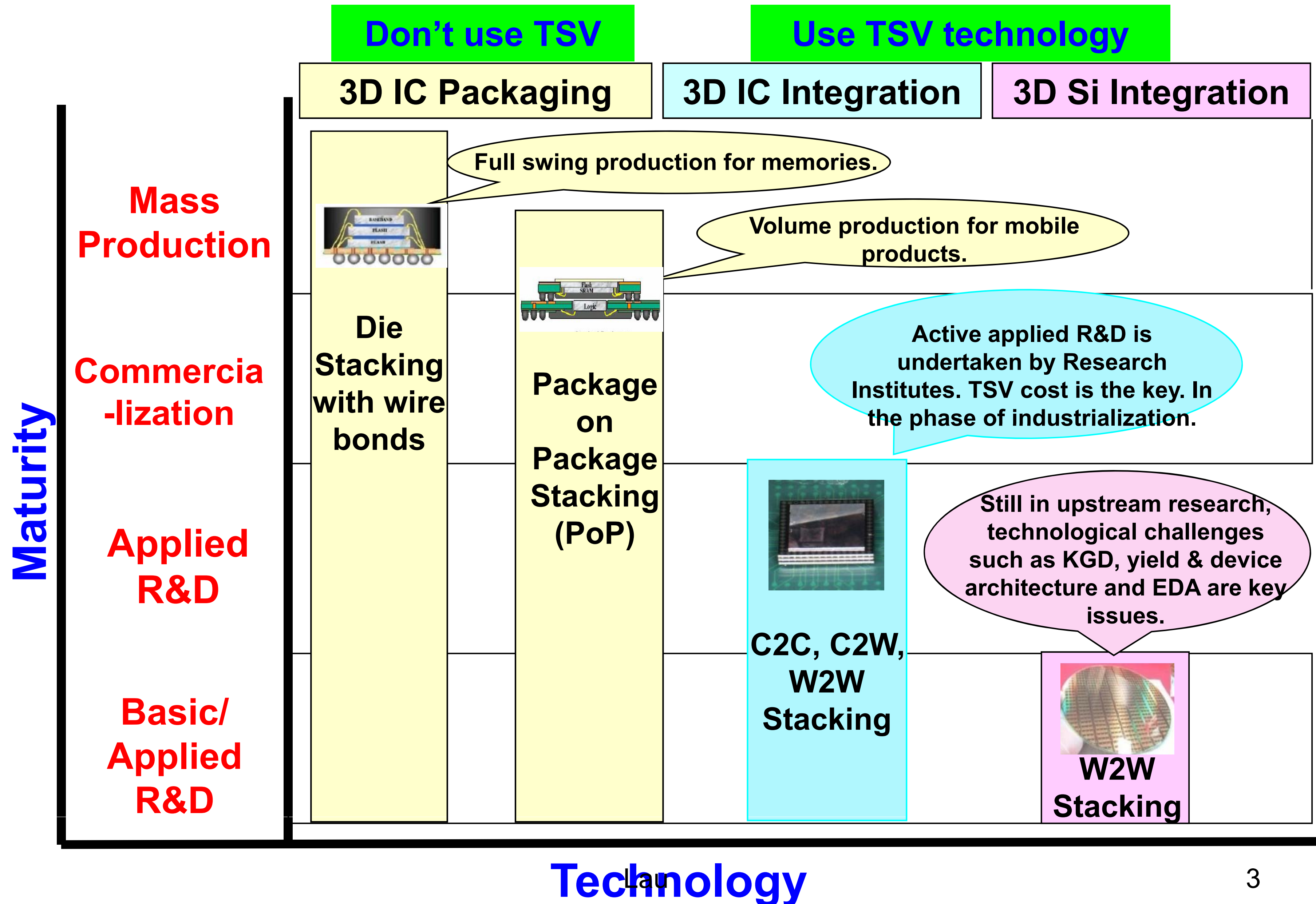
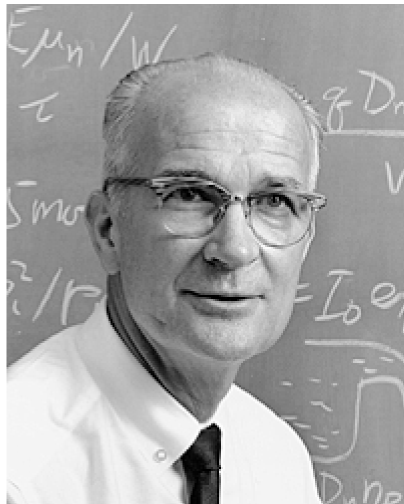
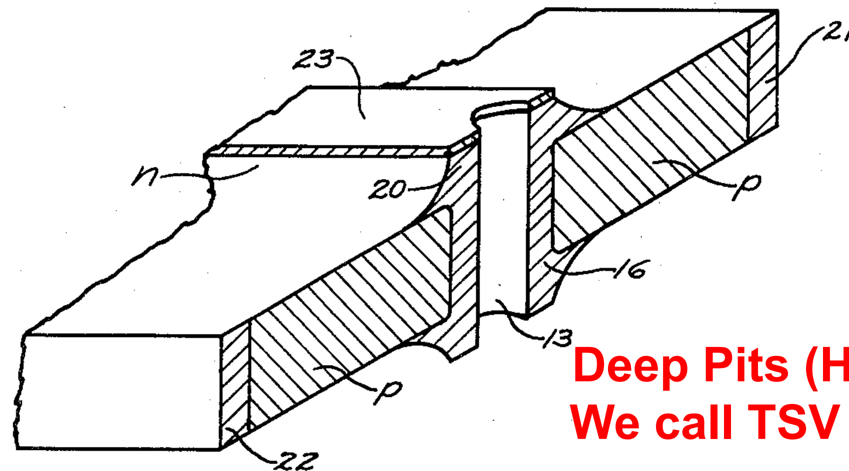
3D Integration Technologies



TSV (Through-Silicon Via)

William Shockley (1956 Nobel laureate, co-invented the transistor) filed a patent, “Semiconductive Wafer and Method of Making the Same” on October 23, 1958 and was granted the US patent (3,044,909) on July 17, 1962.





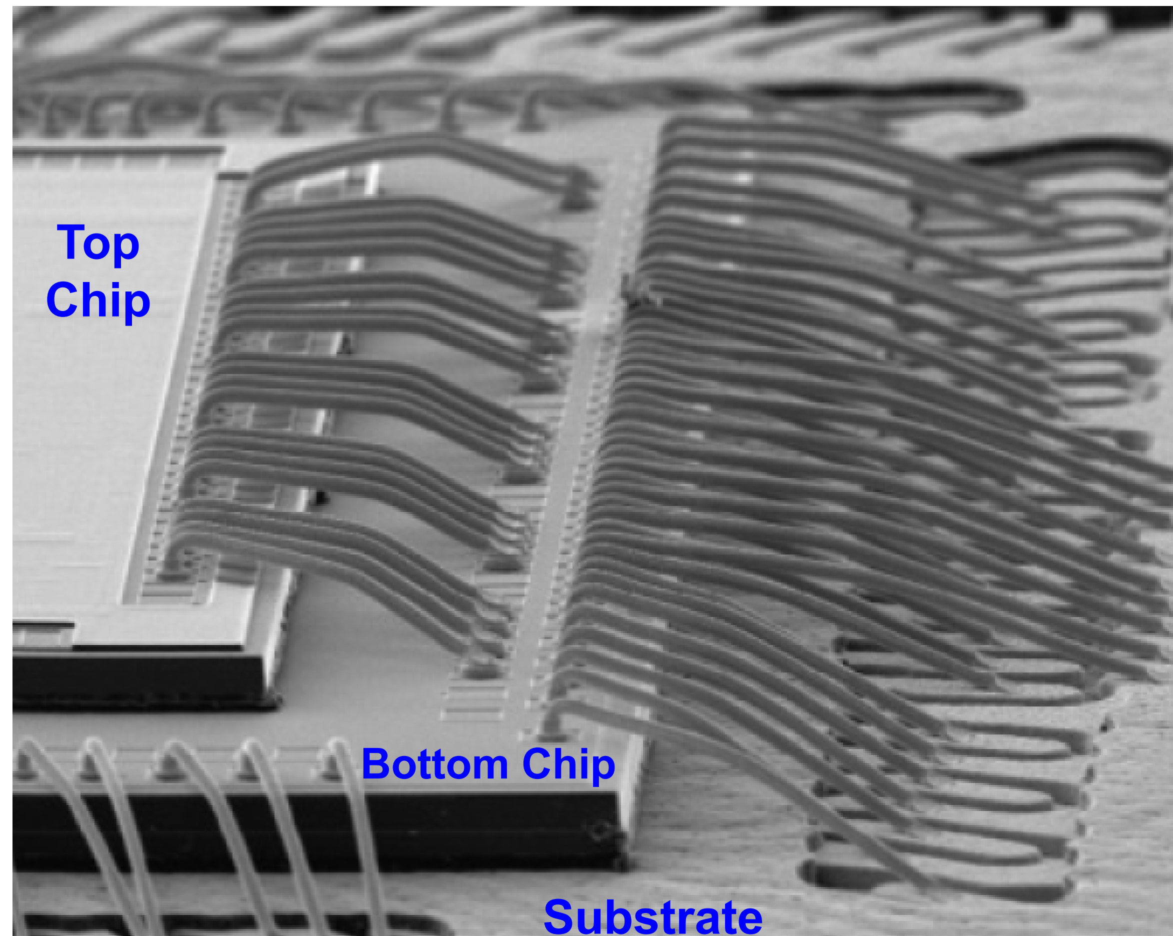
Deep Pits (Holes), We call TSV today

WILLIAM SHOCKLEY
INVENTOR.

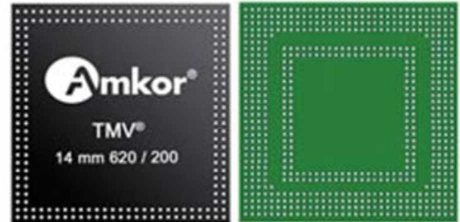
Lau

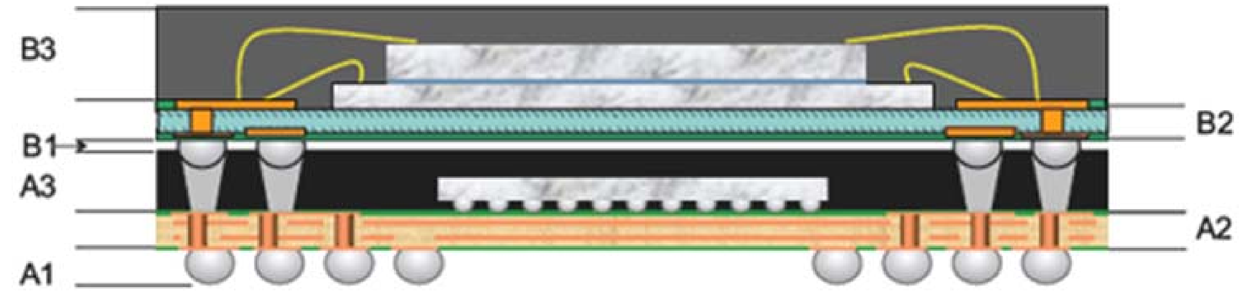
3D IC Packaging (No TSV)

Amkor's 3D IC Packaging with Cu Wires



Amkor's TMV (Thru-Mold Via) PoP (Package-on-Package)





TMV™ PoP Overall Stackup Table

Symbol	Unit	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150
A2 (4L laminate)	mm	0.220	0.300	0.210
A3 (Mold cap)	mm	0.230	0.280	0.250
B1 (Stacked gap)	mm	0.020	0.080	0.050
B2 (2L laminate)	mm	0.100	0.160	0.130
B3 (Mold cap)	mm	0.370	0.430	0.400
Overall Package Height	mm	1.140	1.340	1.240

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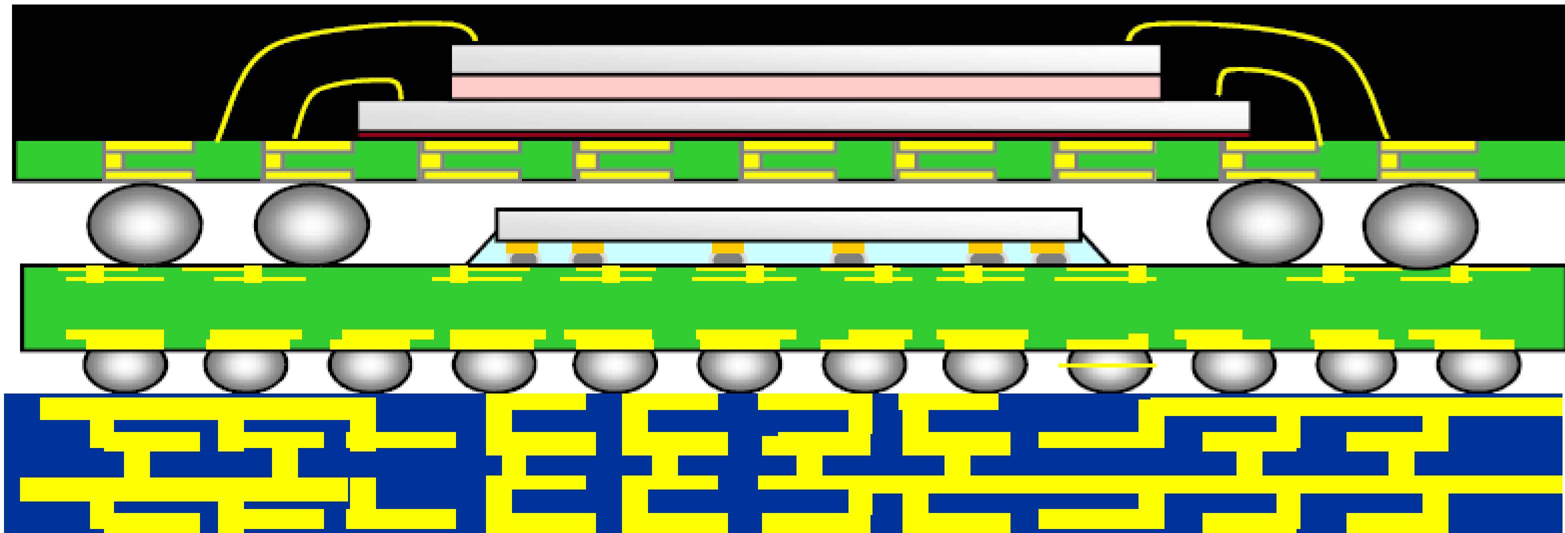
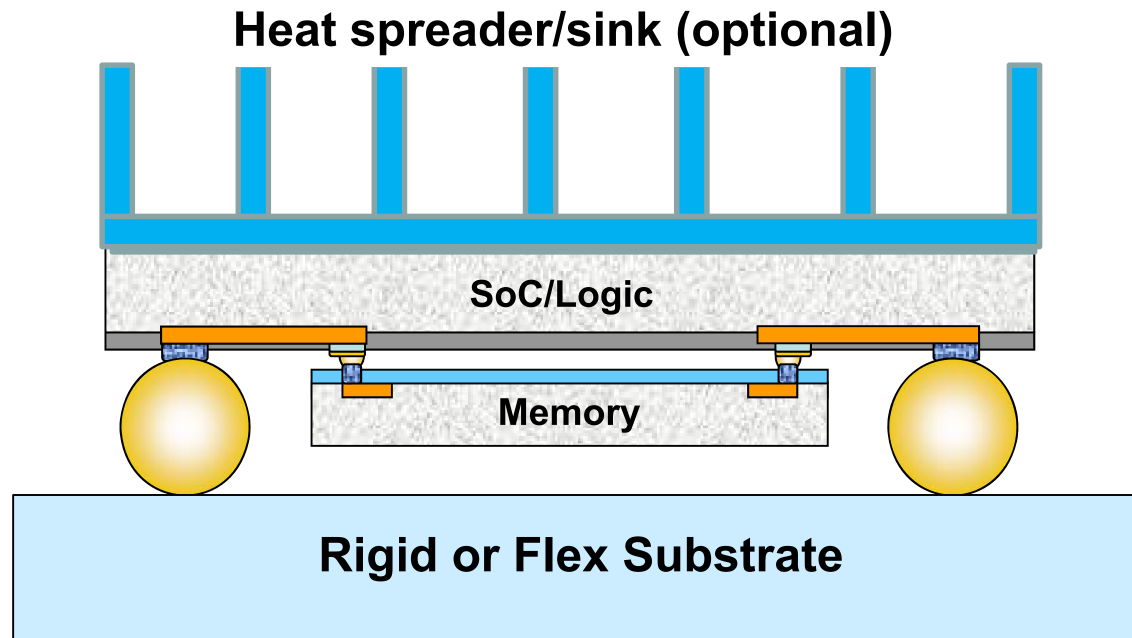
Statschippac's PoP



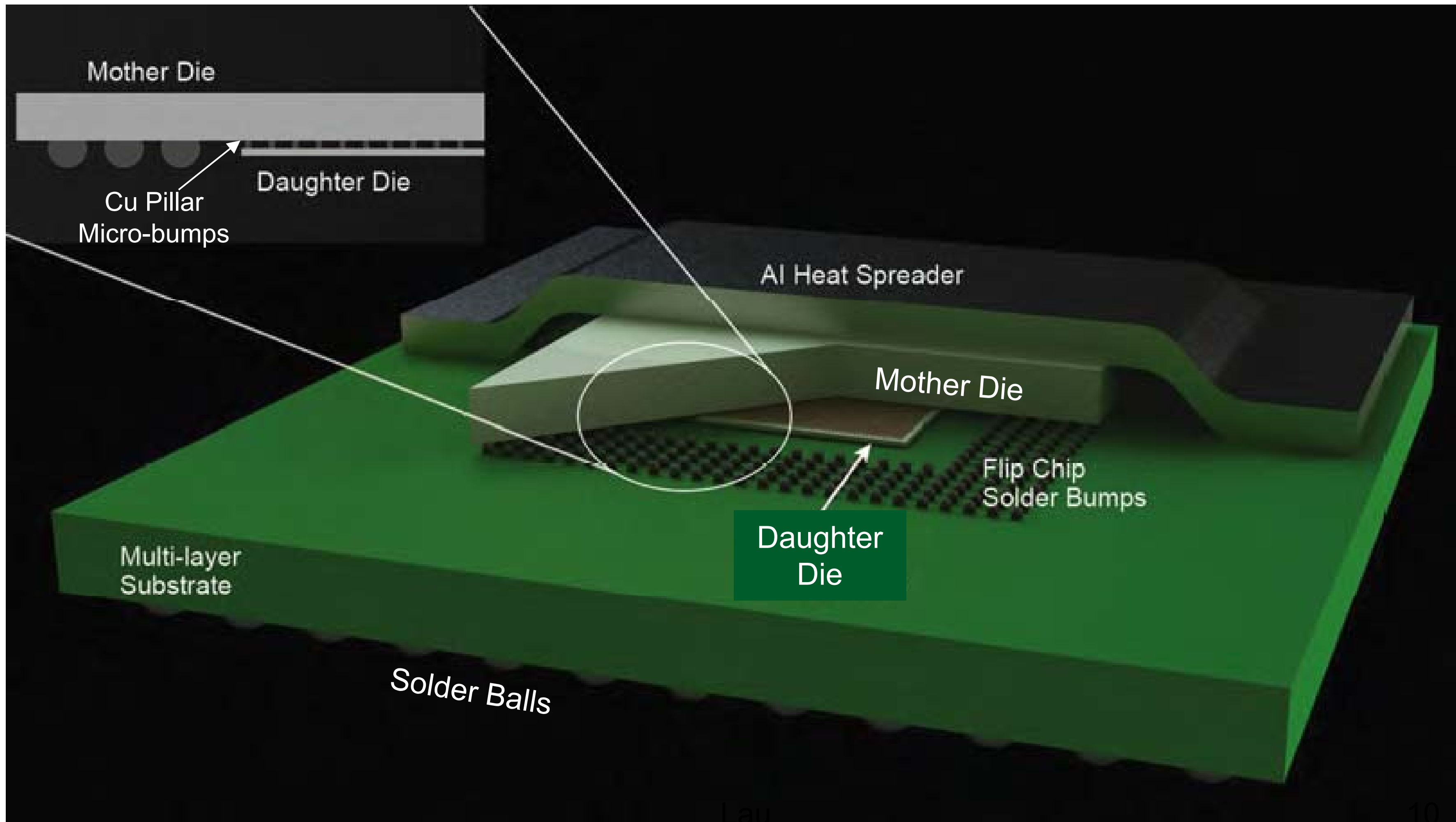
IME's Stacked silicon module attached on a substrate



Chip-to-Chip and Face-to-Face

Lim, Lau, et.al., "Process Development and Reliability of Microbumps", *IEEE Transactions on CPMT*, Vol. 33, 2010, pp. 747-753.

Amkor's POSSUM™ assembly where the daughter die (e.g., memory) is mounted face-to-face with the larger mother die (e.g., SoC). The mother die is then flip chip mounted onto a substrate



(Wide I/O Memory)

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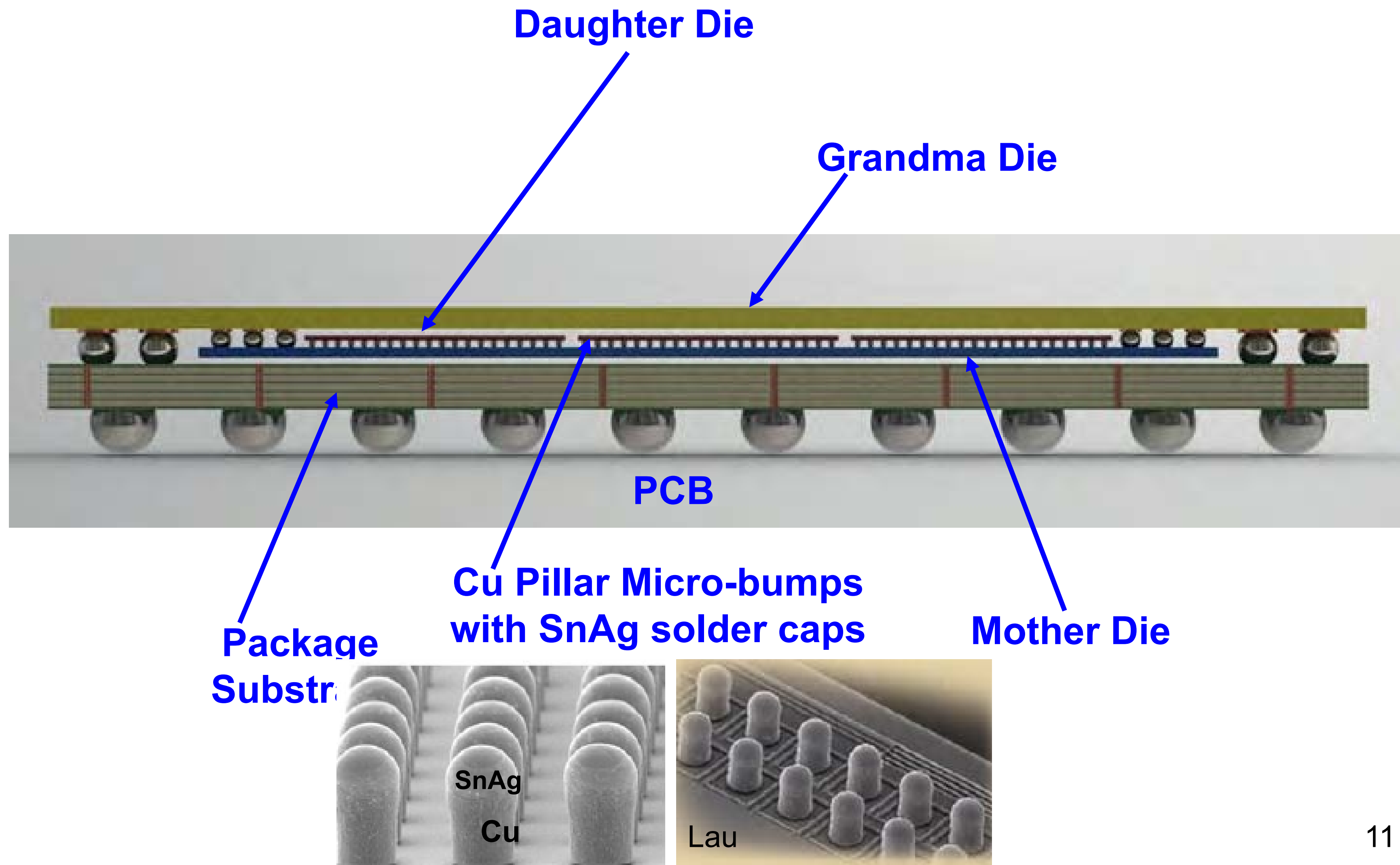
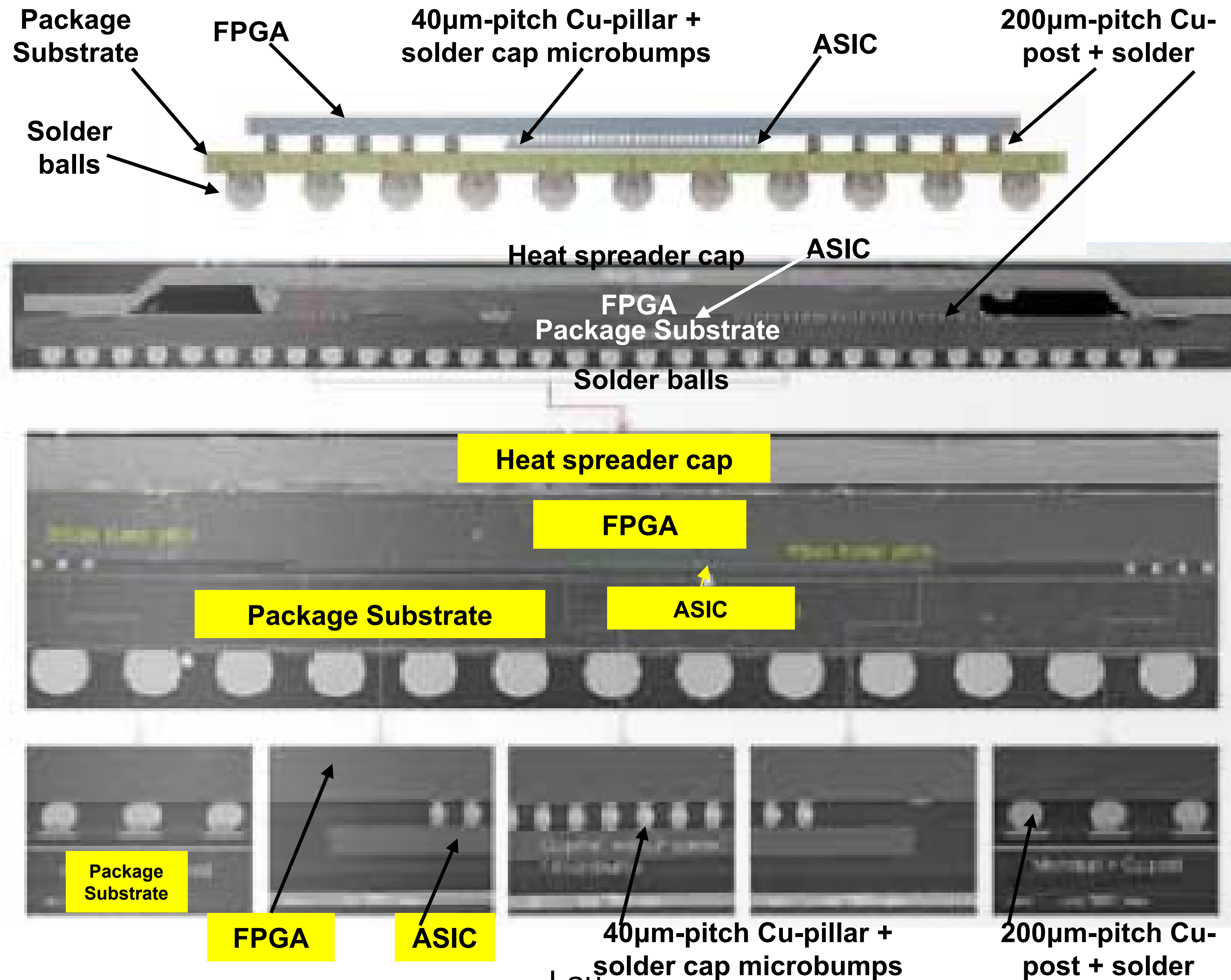
Amkor's Double POSSUM™ multi-stacked die configurations without the use of TSVs

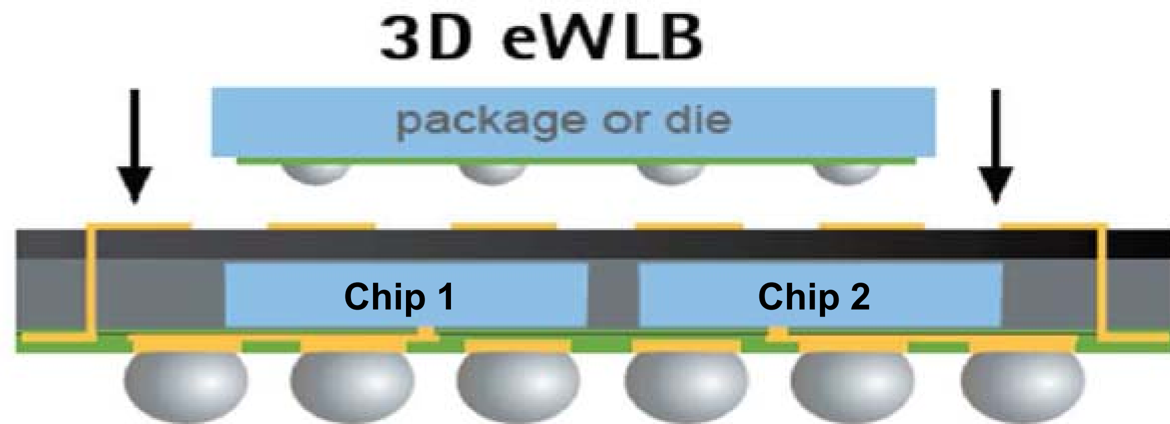


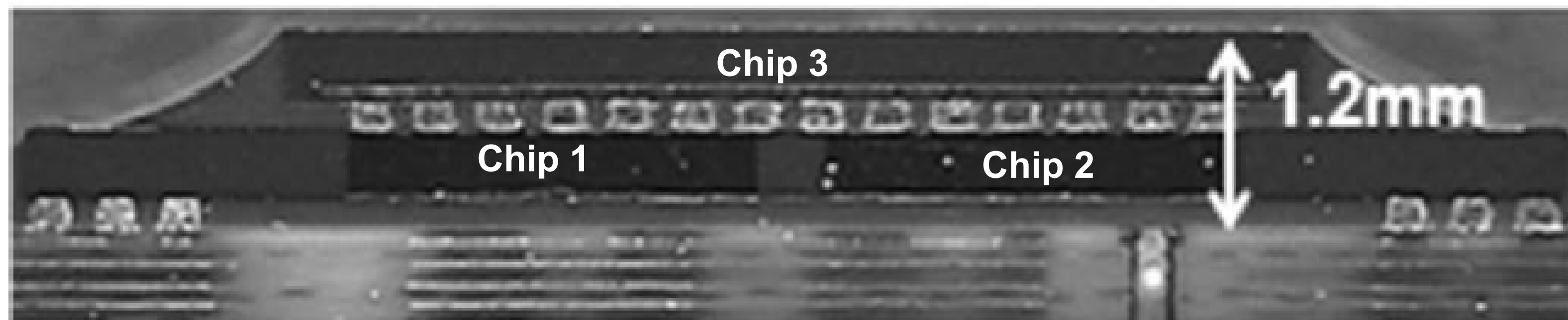
Amkor's POSSUM Package showing Altera's FPGA and ASIC



Xie, J., and D. Patterson, "Realizing 3D IC Integration with Face-to-Face Stacking", Chip Scale Review, May-June Issue, 2013, pp. 16-19.

STMicroelectronics' 3D eWLB

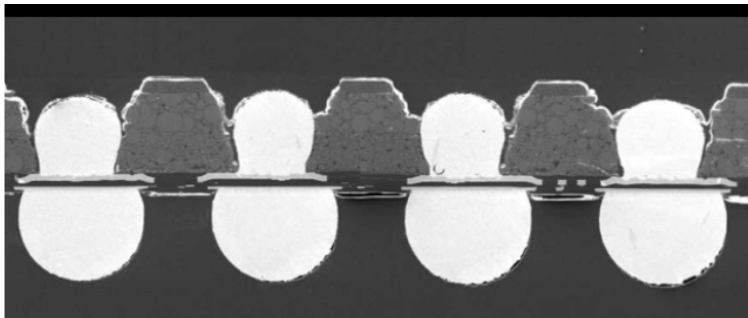




STATSChipPac's 3D IC Packaging

2D
Single chip eWLB
Multi-chip eWLB
eWLL
Flip Chip eWLB
2.5D
2.5D / Extended eWLB
3D
3D eWLB
3D PoP

Top Package
450um
520um
eWLB –PoP Bottom
Si
RDL
450um



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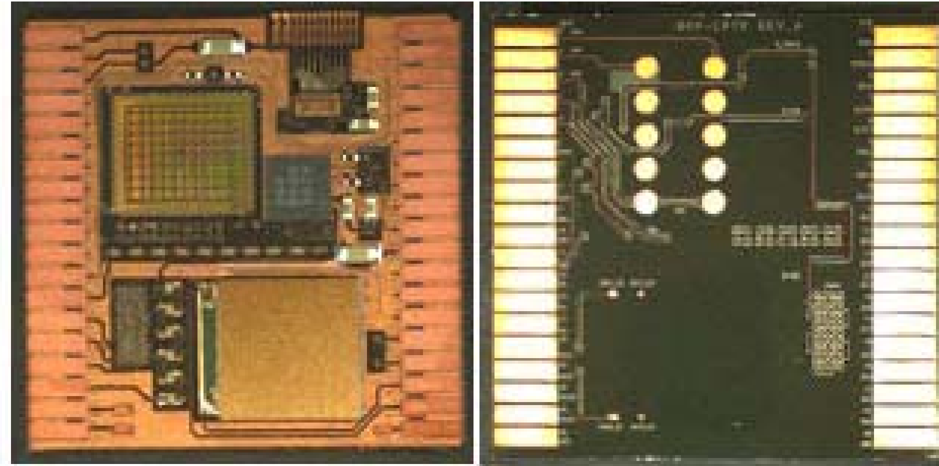
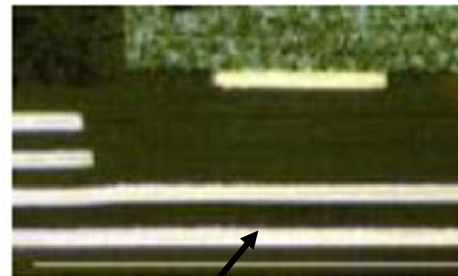
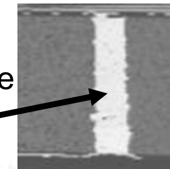
Freescale's 3D IC Packaging





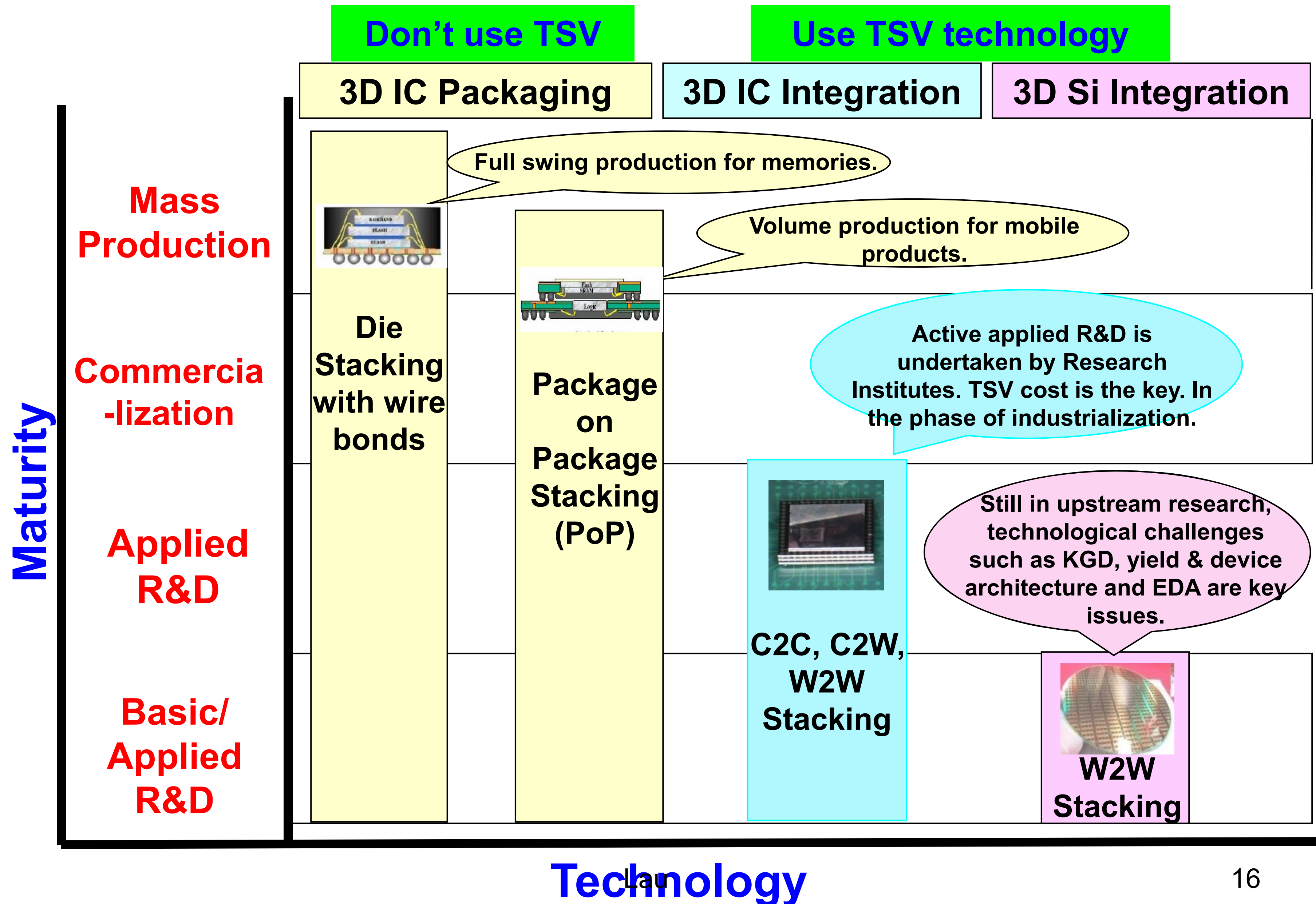
M1
M2
M3
M4



Redistribution layer (RDL)

Through package via (TPV)

3D Integration Technologies

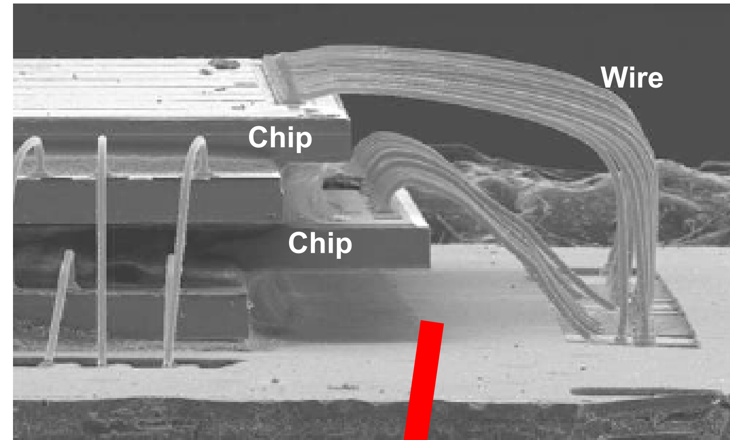


Lau, IEEE-ECTC PDC , 2009

TSV
(Through Silicon Via)
Application Example

Intel's TSV (Through Silicon Via) for the Shortest Chip-to-Chip Interconnects

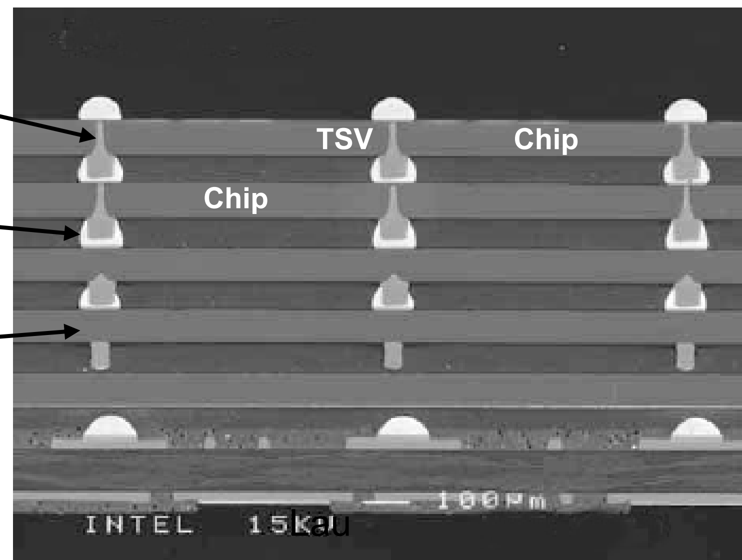
A four stack wire-bonded die package



Wire → TSV

Microbumps

Thin chips



Advantages:

- Smaller form-factor
- Low power consumption
- Wider bandwidth
- Better performance

3D IC Integration

3D IC Integration

3D IC Integration stacks up what ever Moore's law thin chips in the third dimension with TSV and microbumps to achieve performance, lower power, wider bandwidth, small form factor, and eventually low cost!

3D Memory-chip Stacking

Potential Applications of 3D IC Integration

Memory-Chip Stacking

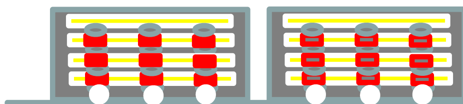
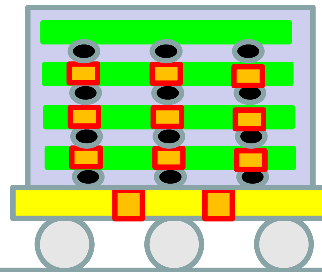
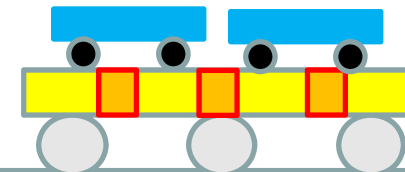
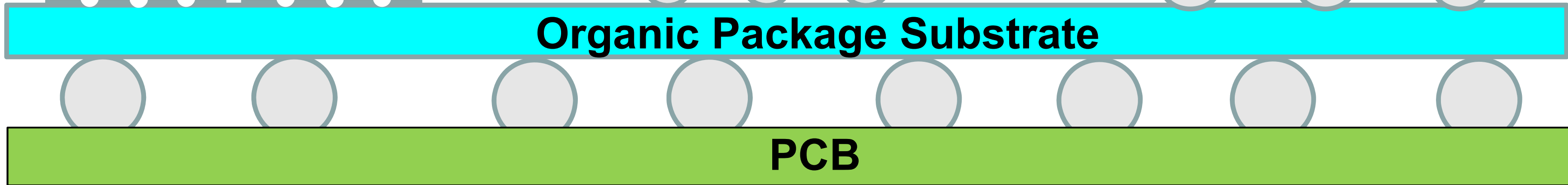
- DRAM or NAND Flash stacking with TSVs on organic substrate
- Over molding the DRAMs or NAND Flash

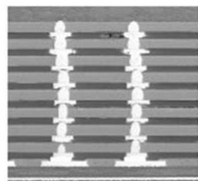
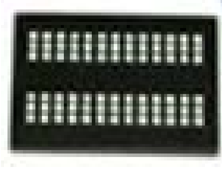
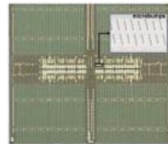
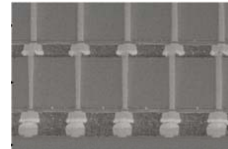
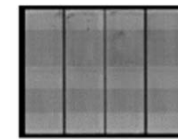
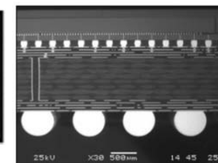
Wide I/O DRAM (Hybrid Memory Cube)

- DRAM stacking with TSVs on Logic Controller with TSVs
- Over molding the DRAMs

Wide I/O Interface (2.5D IC Integration)

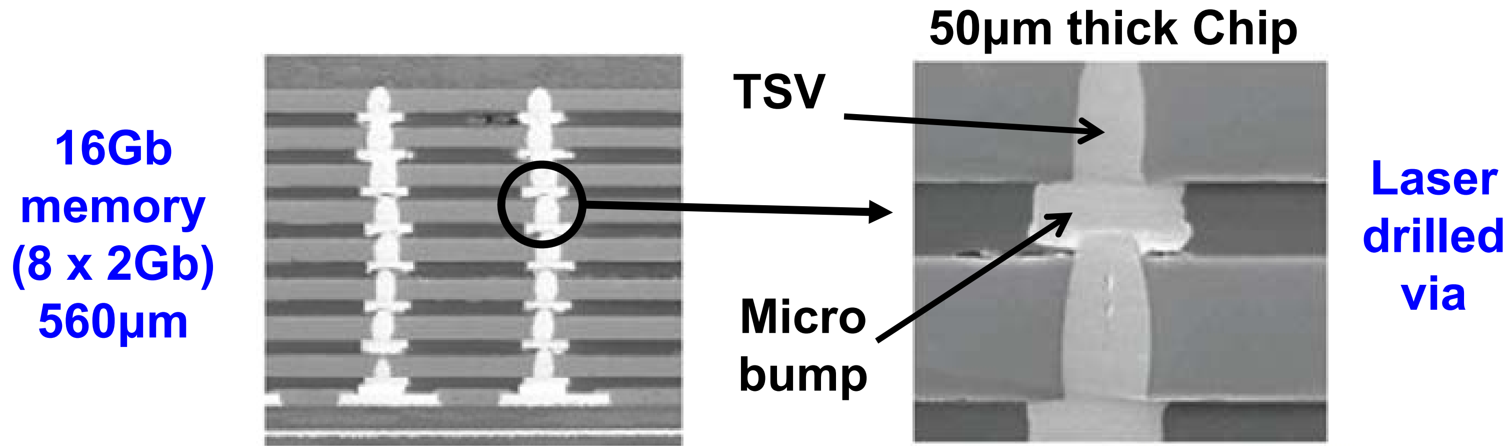
- TSV-less chips on a passive interposer with TSVs
- Underfill is needed between chips and the interposer

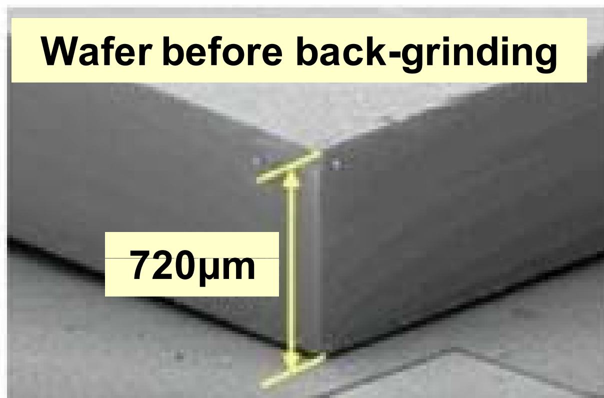





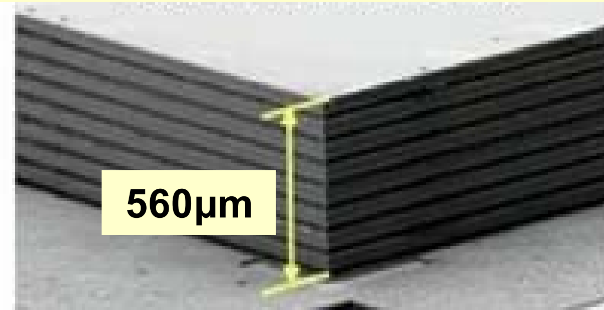







Underfill is needed between the active/passive TSV interposer and the organic substrate

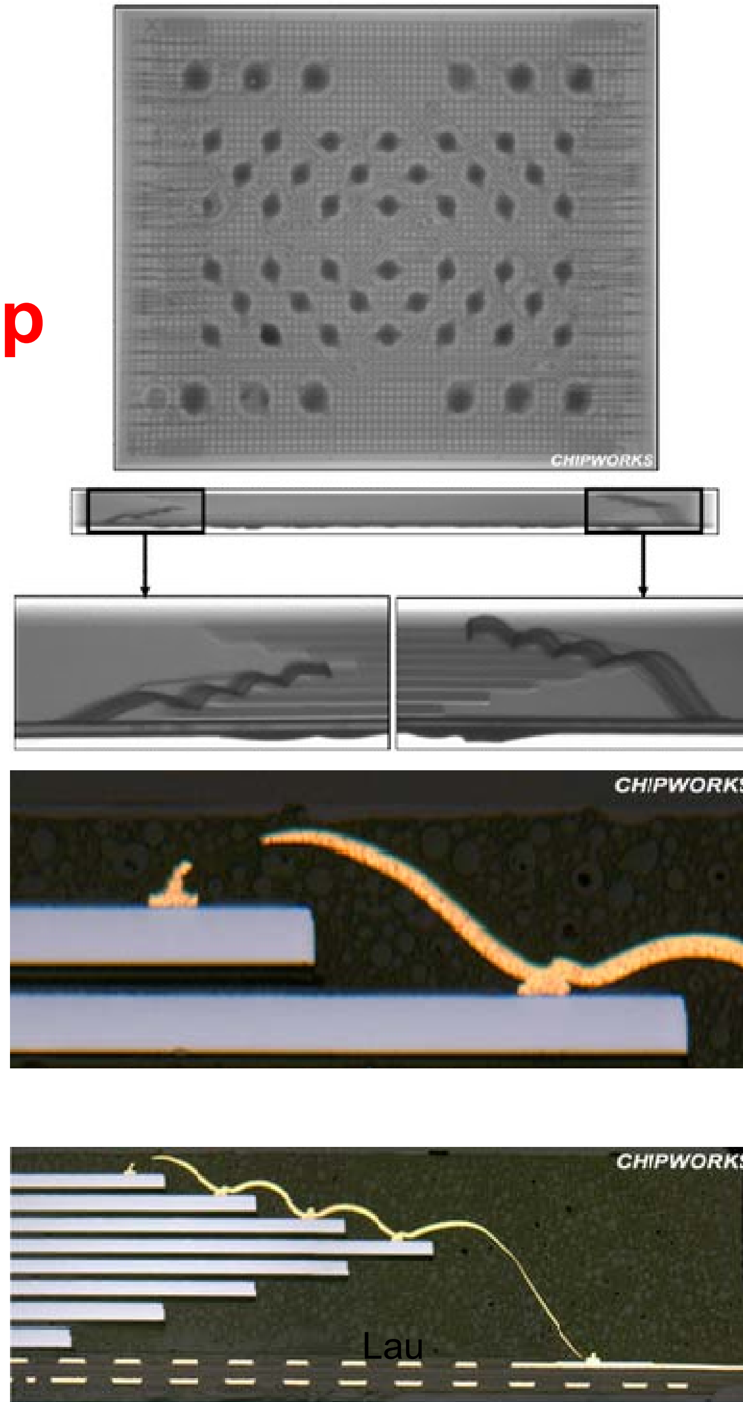
Samsung's 3D Stacking with TSV (Through Silicon Via)







Samsung's Eight-Stack Flash Shows up in Apple's iPhone 4



The package, including substrate, is ~0.93 mm thick, and the die stack is ~670 μm high. Die thicknesses vary from 55 – 70 μm, with the thickest die at the bottom.

Lau, *TSV for 3D Integration*, McGraw-Hill, 2012.

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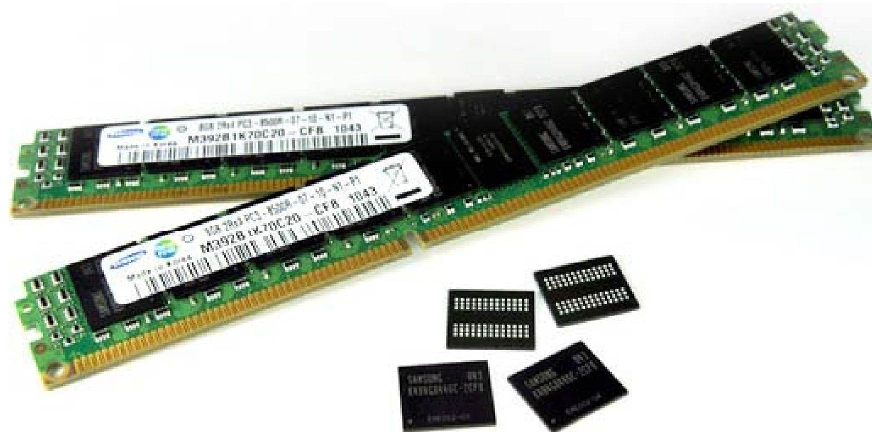
Samsung's 32GB DDR3 registered dual in-line memory modules (RDIMMs) that use TSVs for next-generation servers powered by multi-core chips (8/17/2011)



Server Farm

The new 32GB RDIMM with TSVs and microbumps is based on Samsung's green 4 gigabit (Gb) DDR3 memory made using 30nm technology. It can transmit at speeds of up to 1,333 megabits per second (Mbps), which is a 70% gain over preceding quad-rank 32GB RDIMMs with operational speeds of 800Mbps.

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Wide I/O DRAM (Hybrid Memory Cube)

Lau

Potential Applications of 3D IC Integration

Memory-Chip Stacking

- DRAM or NAND Flash stacking with TSVs on organic substrate
- Over molding the DRAMs or NAND Flash

Wide I/O DRAM (Hybrid Memory Cube)

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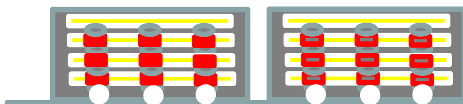
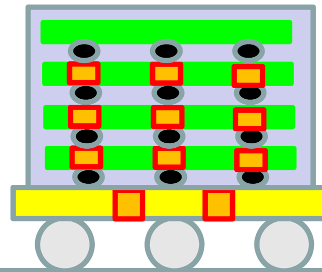
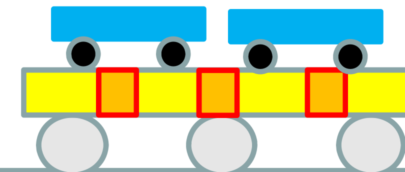
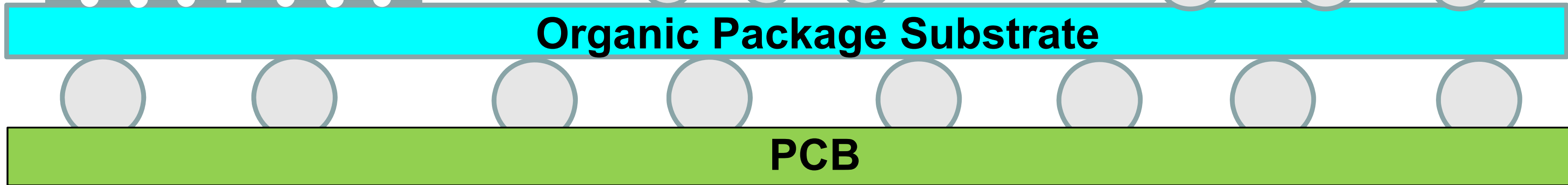
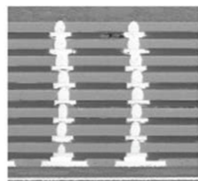
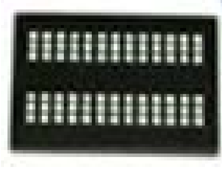
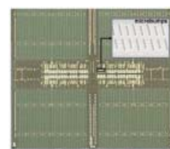
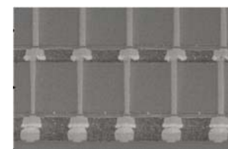
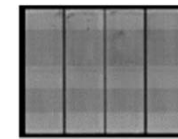
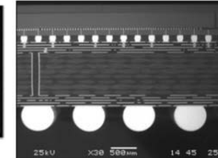
Wide I/O Interface (2.5D IC Integration)

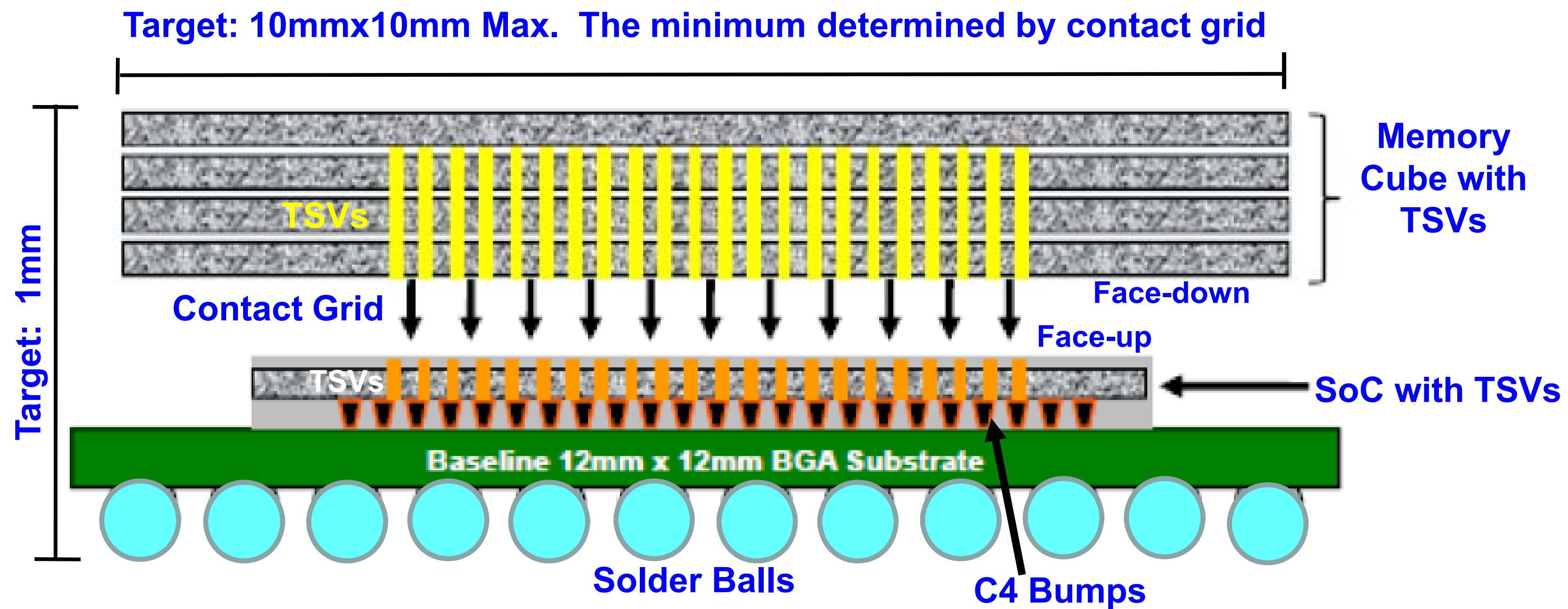
- TSV-less chips on a passive interposer with TSVs
- Underfill is needed between chips and the interposer

Underfill is needed between the active/passive TSV interposer and the organic substrate

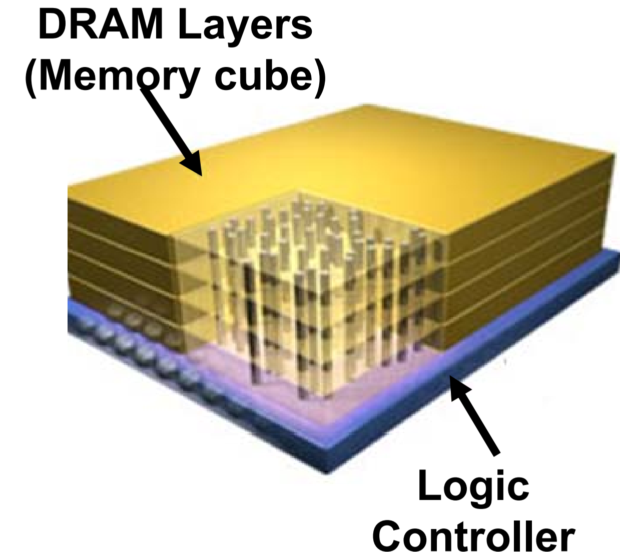
JEDEC Standard (January 2012) Wide I/O DRAM (Micron)



Status of Wide I/O DRAM (Hybrid Memory Cube)

The HMC consortium already has 8 members:

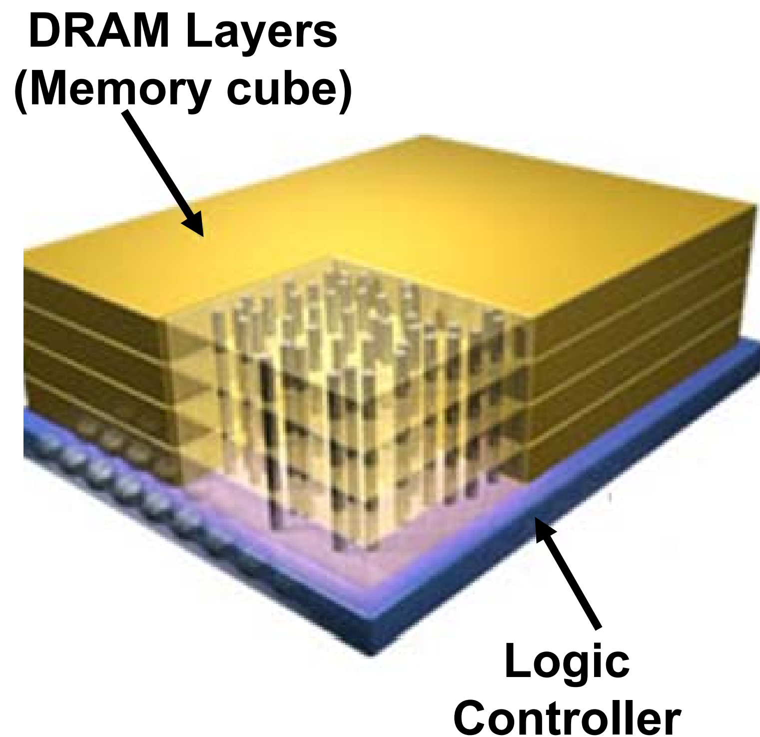
- Micron
- Samsung
- Altera
- ARM
- IBM
- Open-Silicon
- SK Hynix
- Xilinx



The SPEC was published on April 2, 2013 and is primarily targeted at:

- HPC (high performance computing)
- Networking
- Energy,
- Wireless communications
- Transportation
- Security
- High-end servers

Wide I/O DRAM (Hybrid Memory Cube)

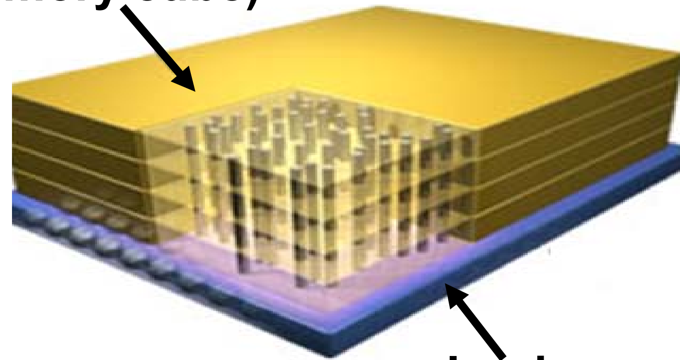


More than 100 developer and adopter members of the hybrid memory cube consortium (HMCC) this week (1st week of April 2013) announced is has reached consensus for the global standard that will deliver a much-anticipated, disruptive memory computing solution. The HMCC is a focused collaboration of OEMs, enablers and integrators who are cooperating to develop and implement an open interface standard for HMC. More than 100 leading technology companies from Asia, Japan, Europe and the U.S. have joined the effort, including:

- Altera
- ARM
- Cray
- Fujitsu
- GlobalFoundries
- HP
- IBM
- Marvell
- Micron Technology
- National Instruments
- Open-Silicon
- Samsung
- SK Hynix
- ST Microelectronics
- Teradyne
- Xilinx

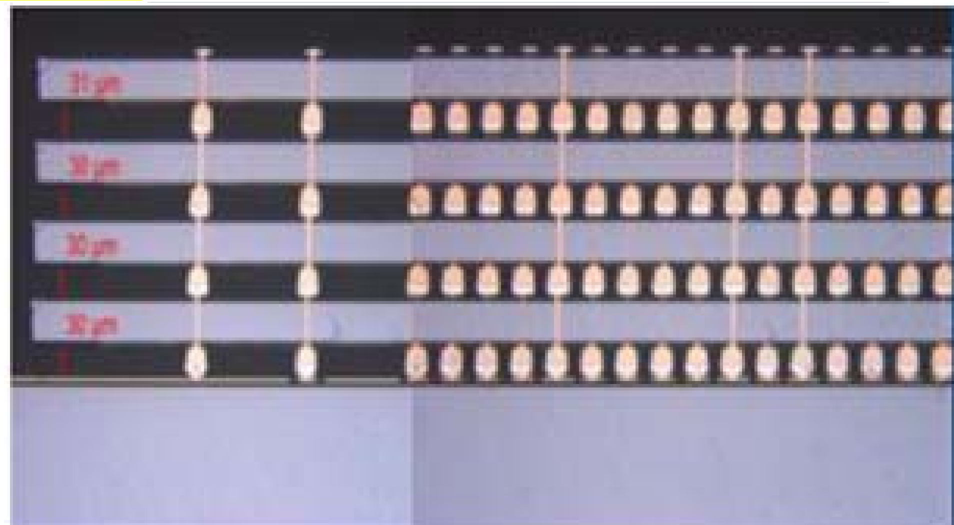
Wide I/O DRAM (Hybrid Memory Cube)

DRAM Layers (Memory cube)

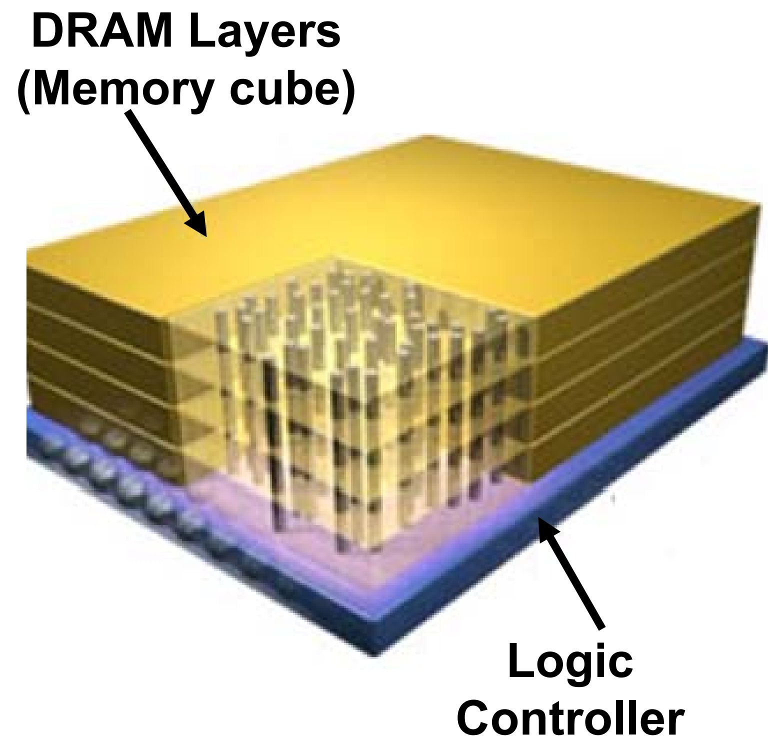


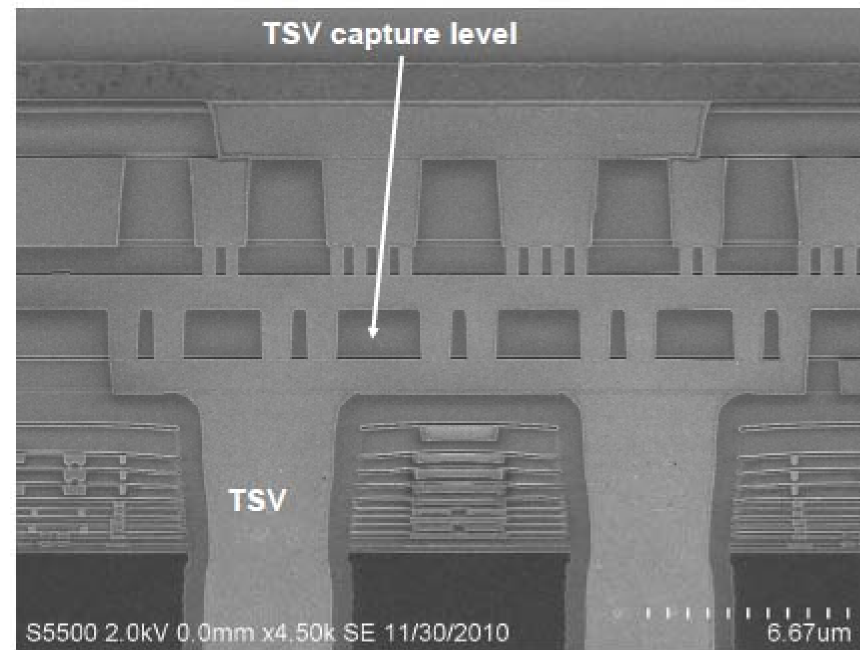
Logic Controller

Micron fabricate the memory cube



Wide I/O DRAM (Hybrid Memory Cube)

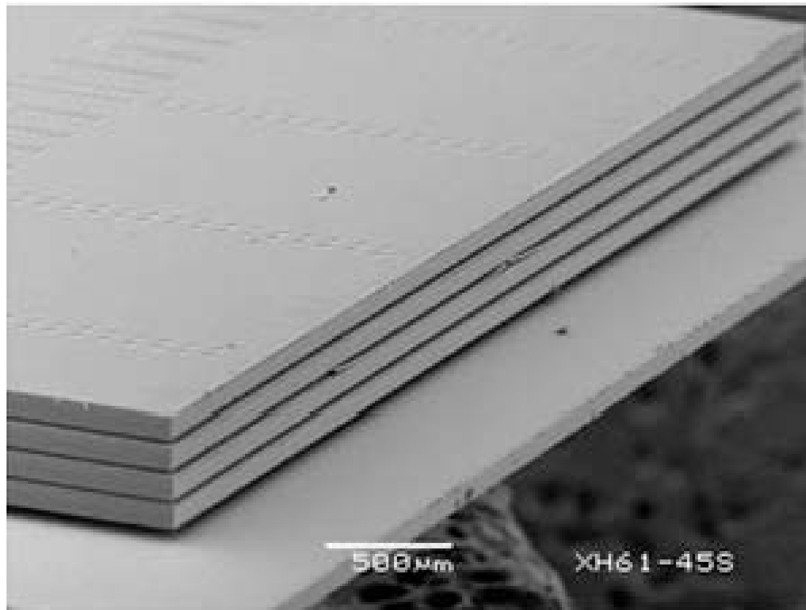




Cross-section SEM showing integrated TSV and BEOL structures (45μm)

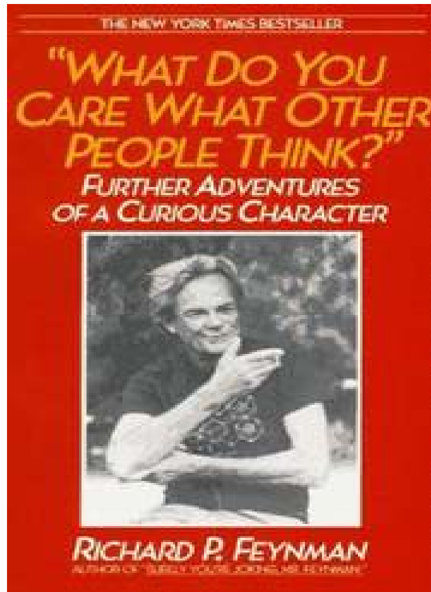
IBM fabricate the Logic Controller

HMC Samples



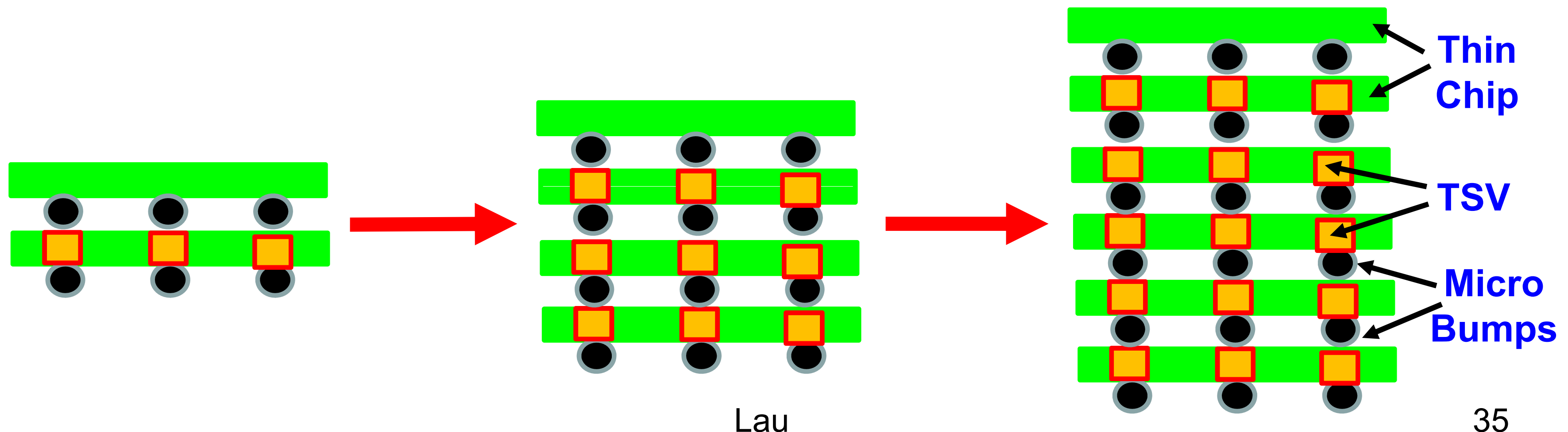
HMC Samples

3D IC Integration (The right thing to do!)

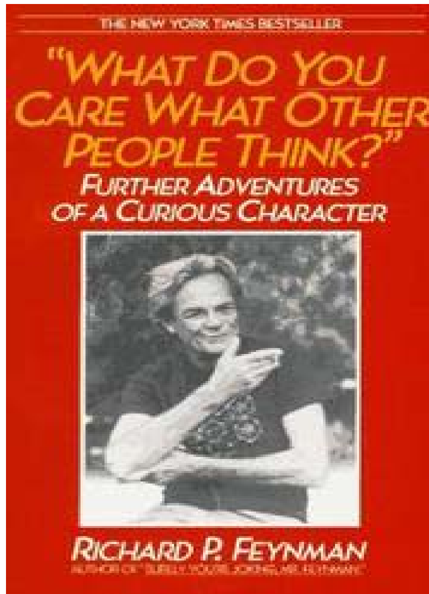


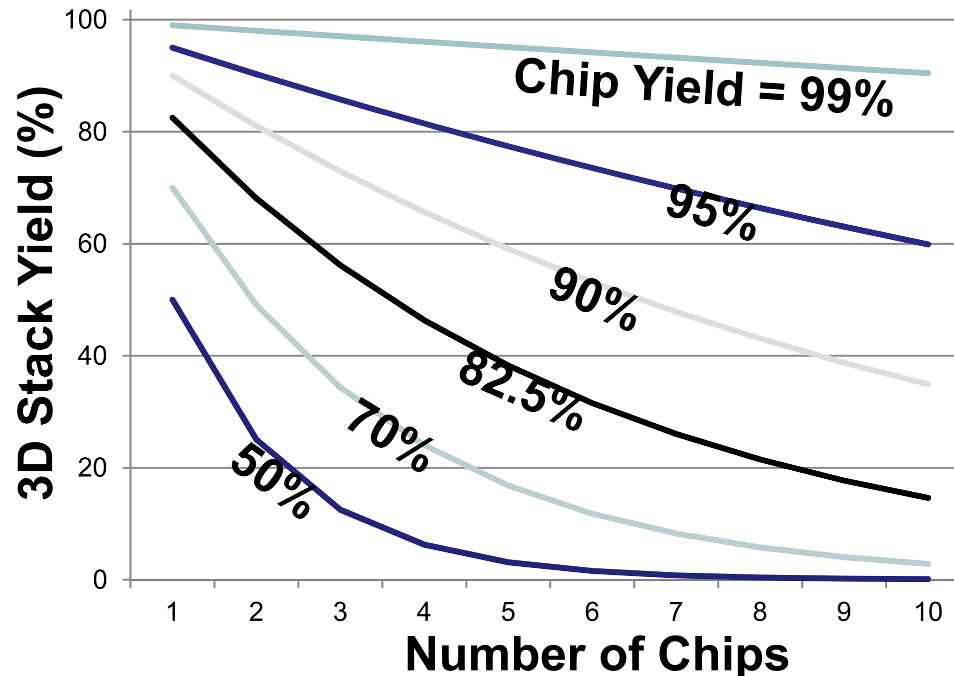
Said the 1965 Nobel Physics laureate, Richard Feynman at the Gakushuin University (Tokyo) in 1985:

"Another direction of improvement (of computing power) is to make physical machines three dimensional instead of all on a surface of a chip (2D). That can be done in stages instead of all at once – you can have several layers and then add many more layers as time goes on."



3D IC Integration (Known Good Die)

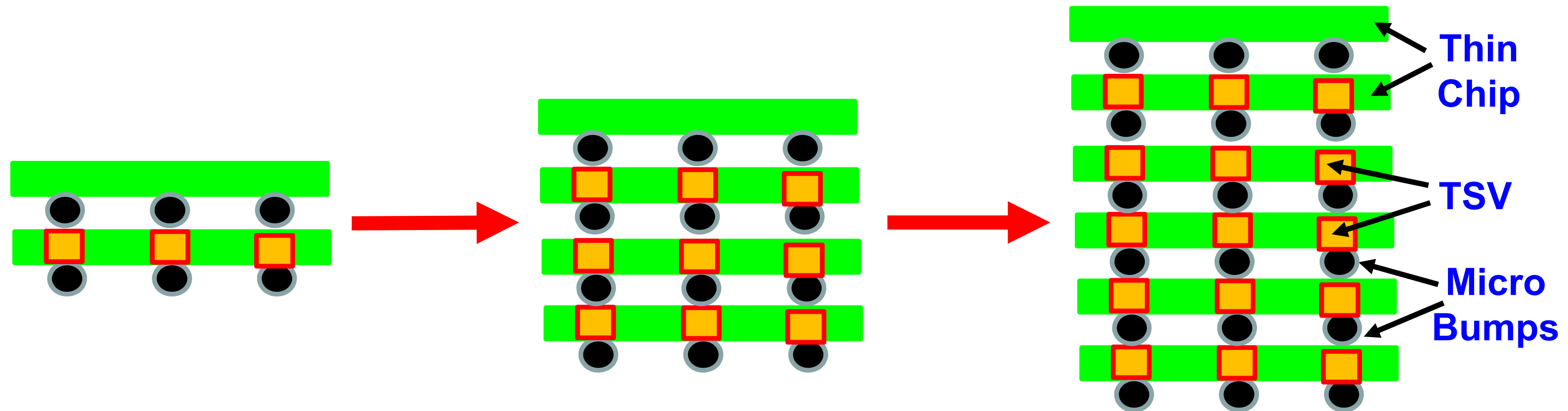




Feynman went on to say: "Another important device would be a way of detecting automatically defective elements (BIST) on a chip, then this chip itself automatically rewiring itself so as to avoid the defective elements (BISR)."

BIST (Build-in self test)
BISR (Build-in self repair)

3D IC Integration (The right thing to do!)



TSVs straight through the same memory chips to:

- ◆enlarge the memory capacity
- ◆lower the power consumption
- ◆increase the bandwidth
- ◆reduce the form factor

will be the major applications of 3D IC Integration!

Who Makes the TSV for Device Wafers?

Memory and Logic Controller are with devices such as the transistors.

For device wafers of 3D IC integration applications, the TSVs are better fabricated by the via-middle process, i.e., after the FEOL to make the devices and MOL to make the metal contacts, but before the BEOL to make the metal layers.

Also, the TSVs should be fabricated by the FAB, where all the equipment and expertise are already exist and the cost to fabricate the TSVs is less than 5% of the cost in fabricating the (≦32nm) device wafers!

Wide I/O Interface

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Potential Applications of 3D IC Integration

Memory-Chip Stacking

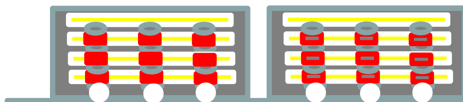
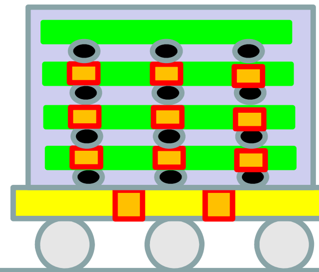
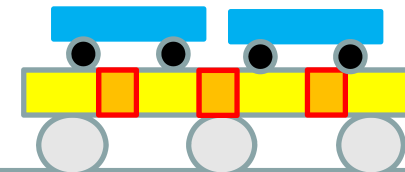
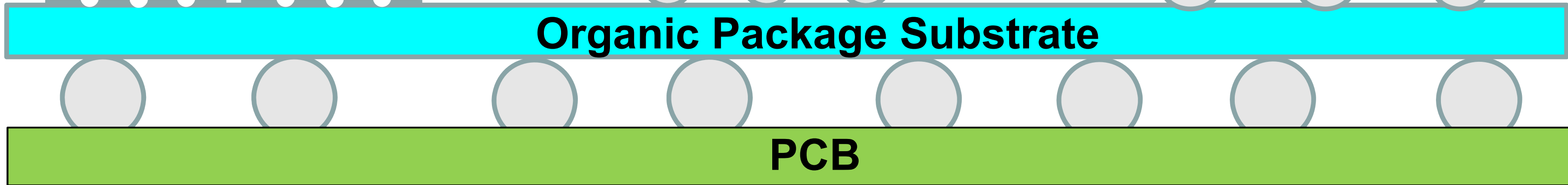
- DRAM or NAND Flash stacking with TSVs on organic substrate
- Over molding the DRAMs or NAND Flash

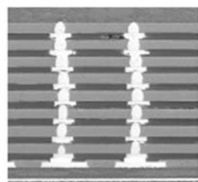
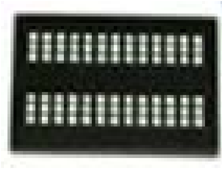
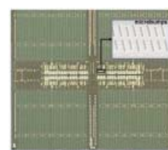
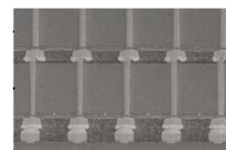
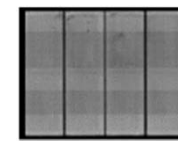
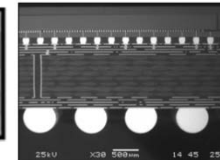
Wide I/O DRAM (Hybrid Memory Cube)

- DRAM stacking with TSVs on Logic Controller with TSVs
- Over molding the DRAMs

Wide I/O Interface (2.5D IC Integration)

- TSV-less chips on a passive interposer with TSVs
- Underfill is needed between chips and the interposer

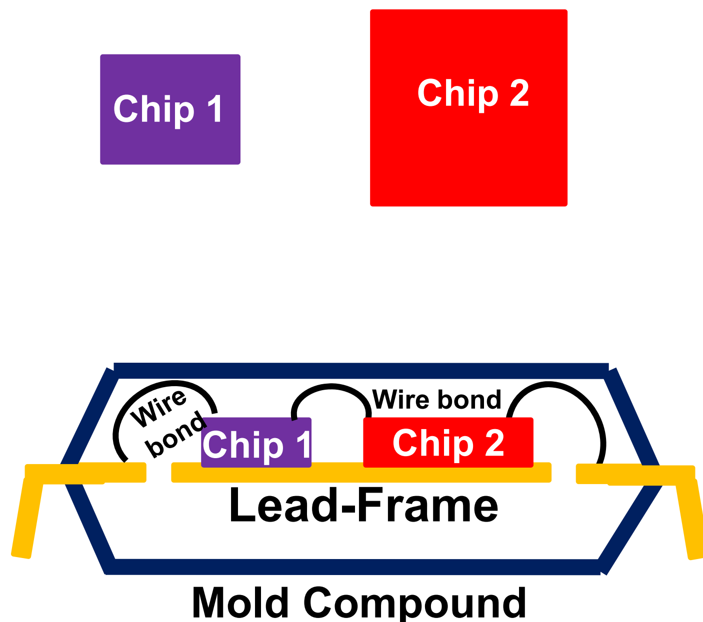
Underfill is needed between the active/passive TSV interposer and the organic substrate

2.5D Passive Interposer

Package Hierarchy and Co-Design

Given:

- Chip Size
- Pin-outs
- Pad size
- Pad-pitches
- On-chip Performance
- Power dissipation
- Etc.



Design for:

◆Cost, size/weight, Performance, and reliability for Consumer / Portable products

◆Performance, reliability, power, and cost for Computer / Internet products

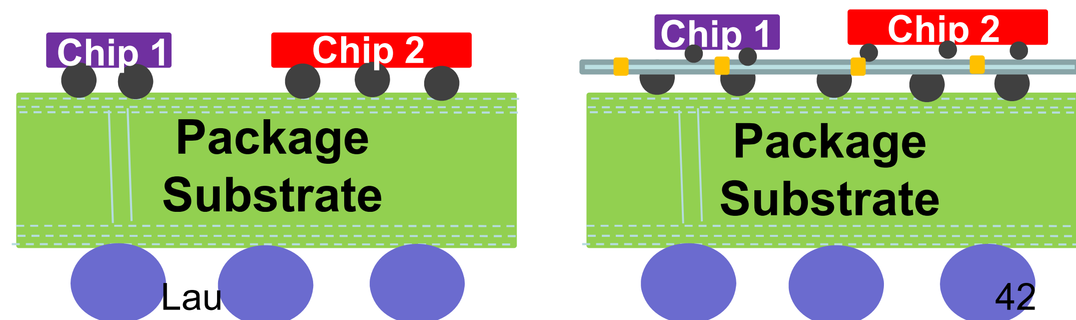
◆Reliability, cost, and performance for Automotive products

◆Reliability, performance, and cost for Military products

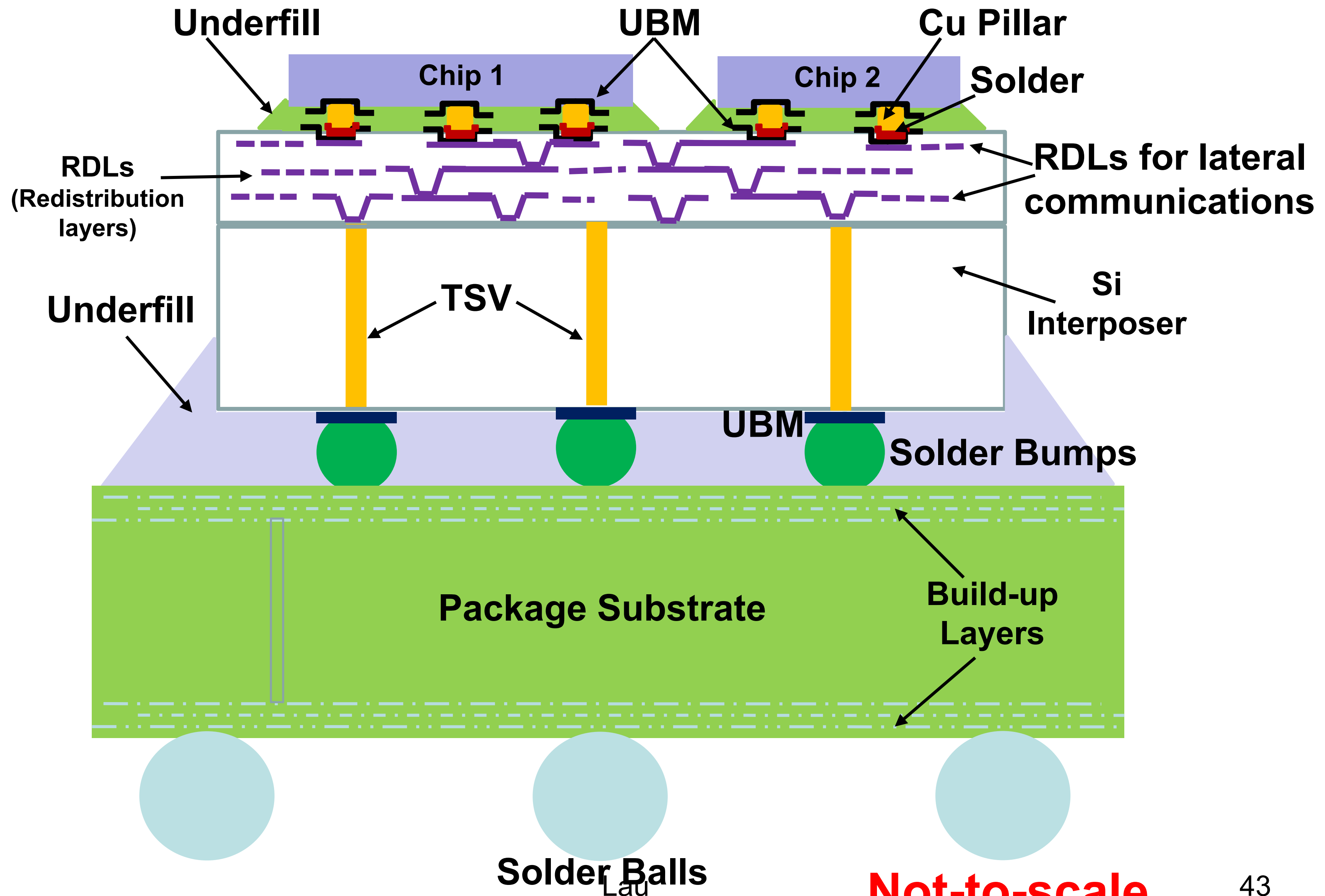
To Meet:

➢Off-chip performance

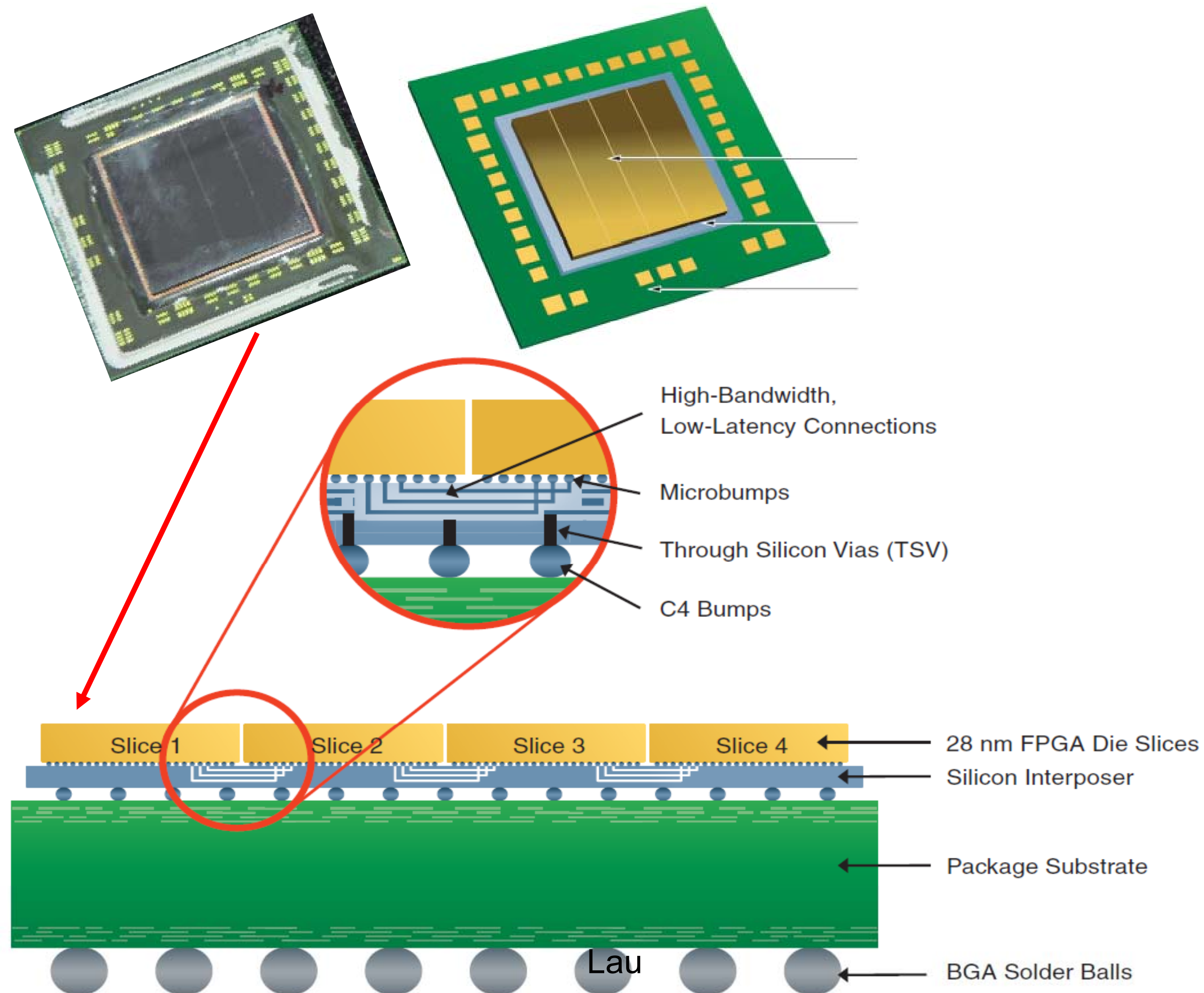
➢Maximum junction temperature, etc.



2.5D IC Integration (Interposers)



Xilinx's Passive Interposers with TSV for Wide I/O Interface in FPGA Products

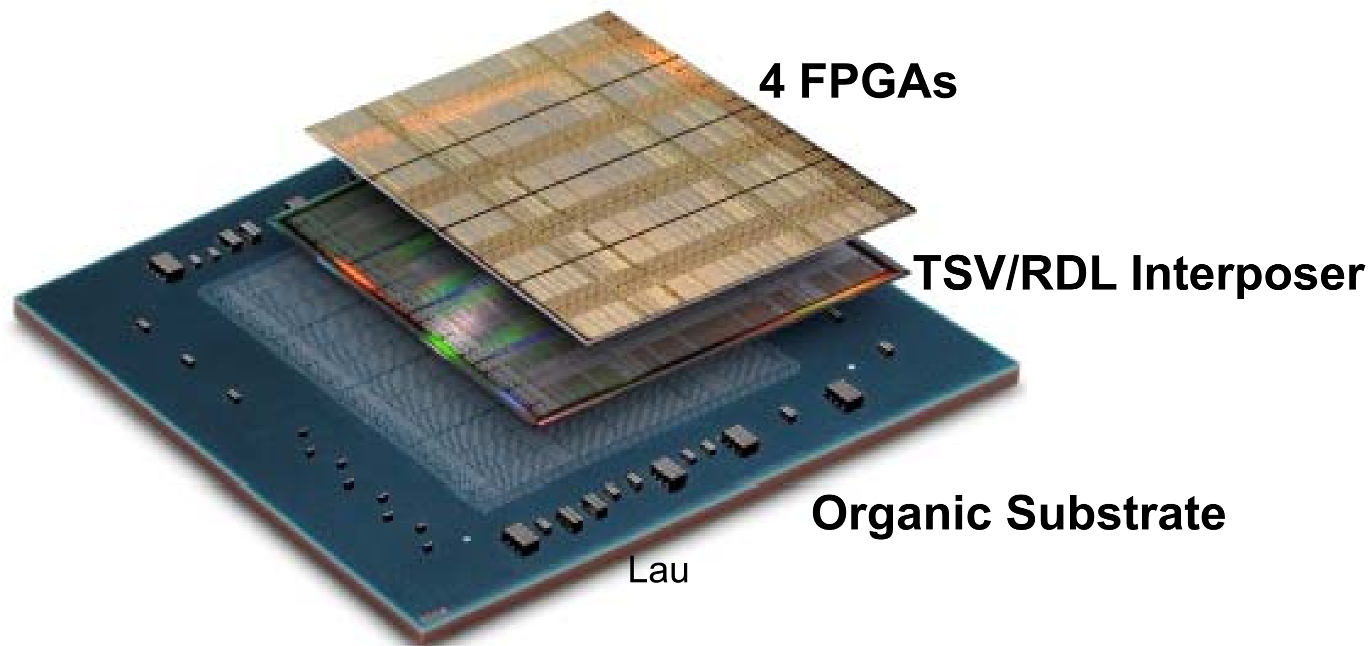


Xilinx's Virtex-7 2000T is Homogeneous

(because all four FPGA dice are identical)

The Virtex-7 2000T is currently the world's highest-capacity programmable logic device – it contains 6.8 billion transistors, providing designers with access to 2 million logic cells. This is equivalent to 20 million ASIC gates, which makes these devices ideal for system integration, ASIC replacement, and ASIC prototyping and emulation.

The capacity is made possible by Xilinx's Stacked Silicon Interconnect technology. This involves a special layer of silicon known as a "silicon interposer" combined with through-silicon vias (TSVs). In the case of the Virtex-7 2000T, four FPGA dice are attached to the silicon interposer, which – in addition to connecting the FPGAs to each other (~10,000 connections between adjacent dice) – provides connections to the chip package.



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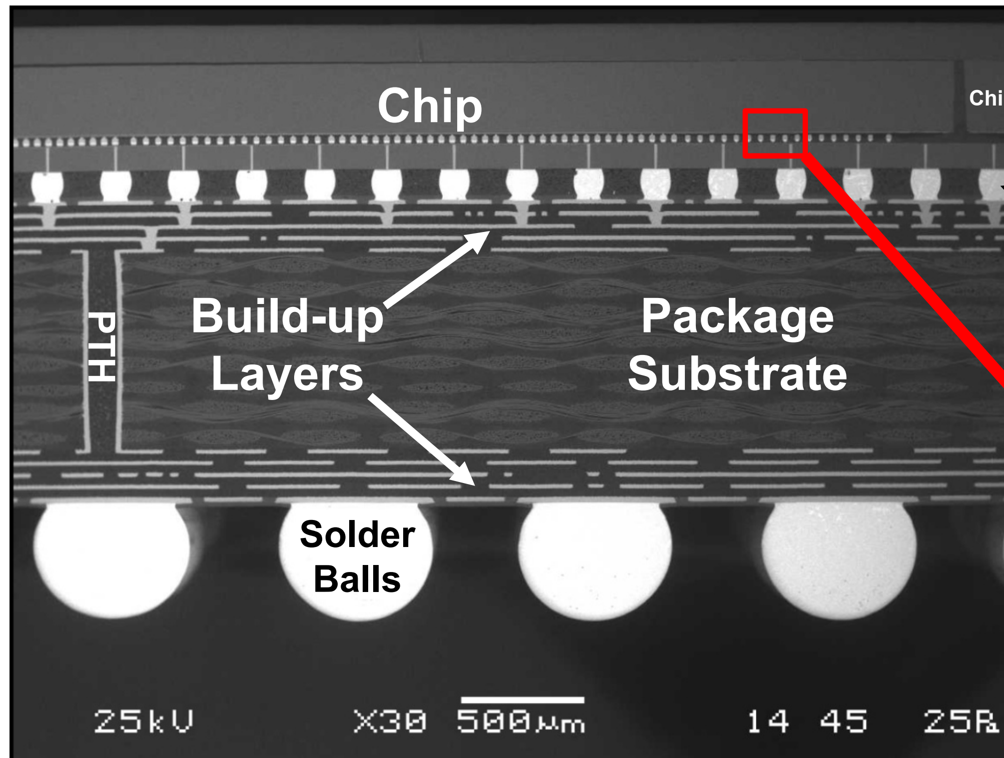
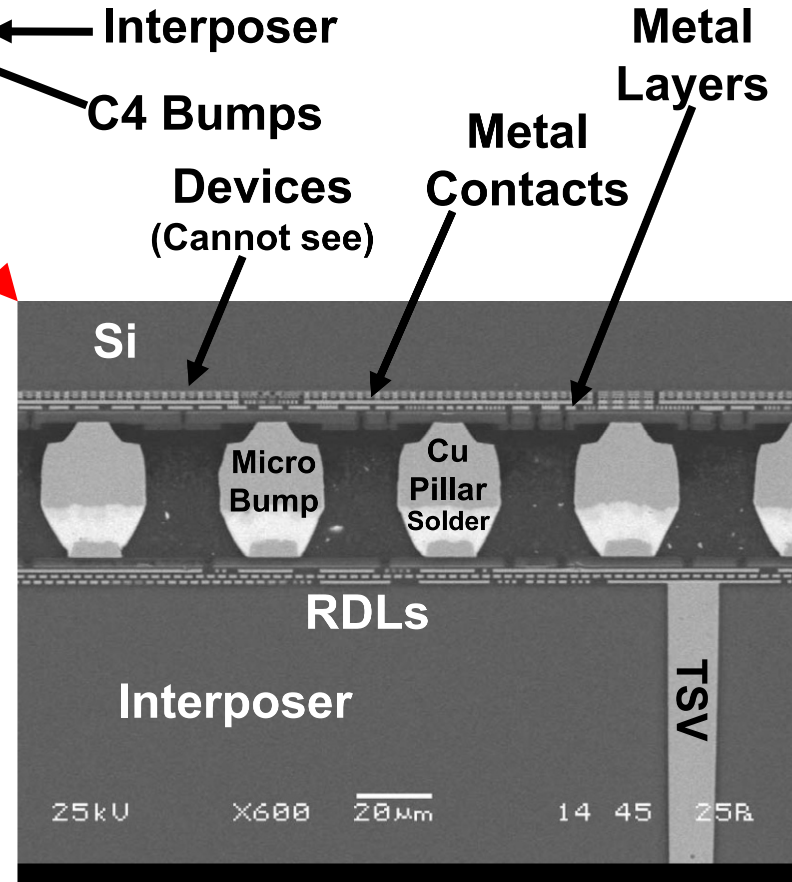
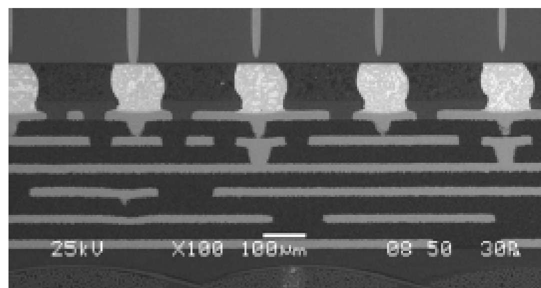
Xilinx/TSMC's 2.5D IC Integration with FPGA



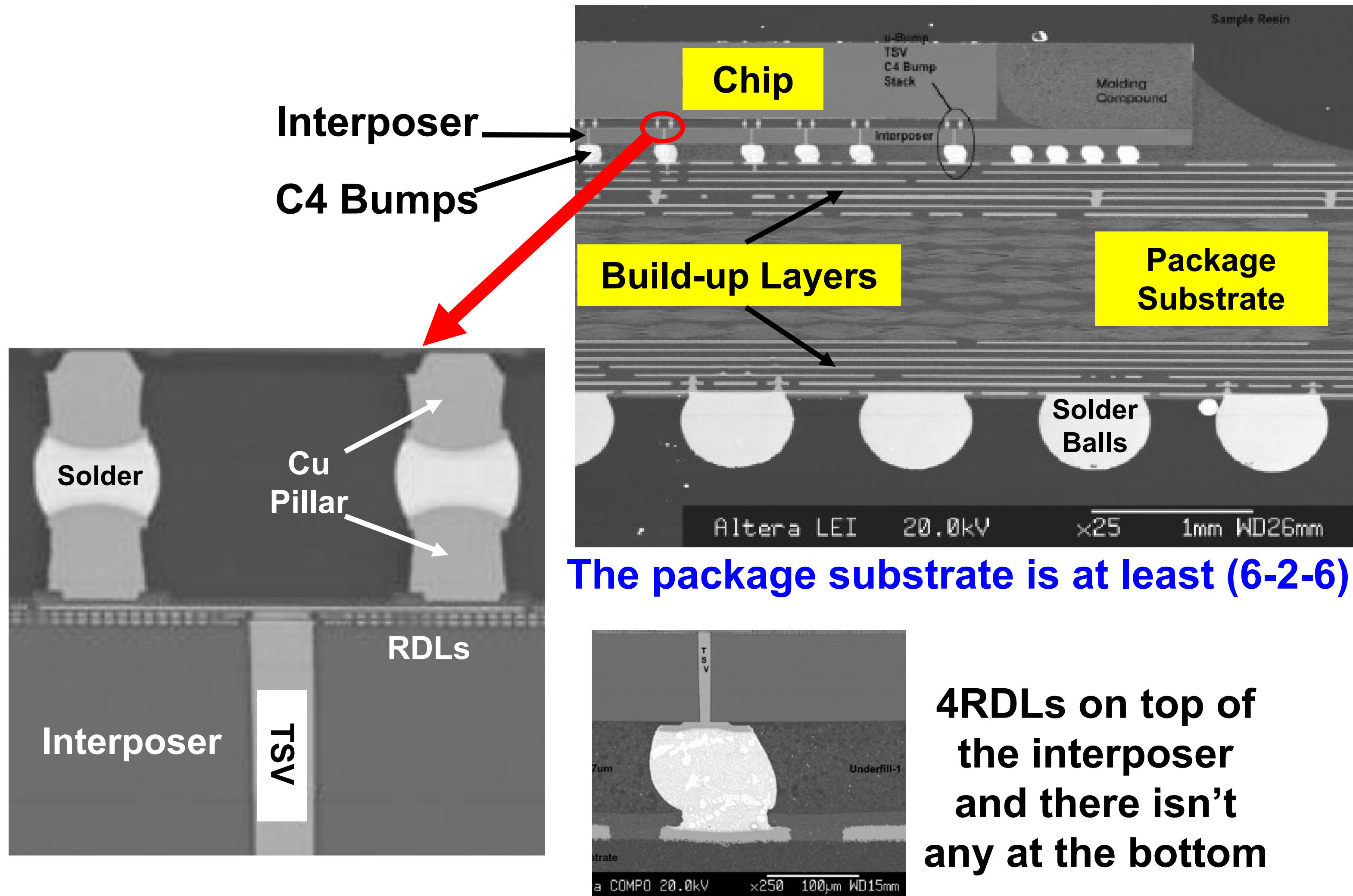




The package substrate is at least (5-2-5)

RDLs: line width and spacing are at 0.4µm pitch

Altera/TSMC's 2.5D IC Integration with FPGA



The package substrate is at least (6-2-6)

4RDLs on top of the interposer and there isn't any at the bottom

Re-distribution Layer (RDL) in Future Packages

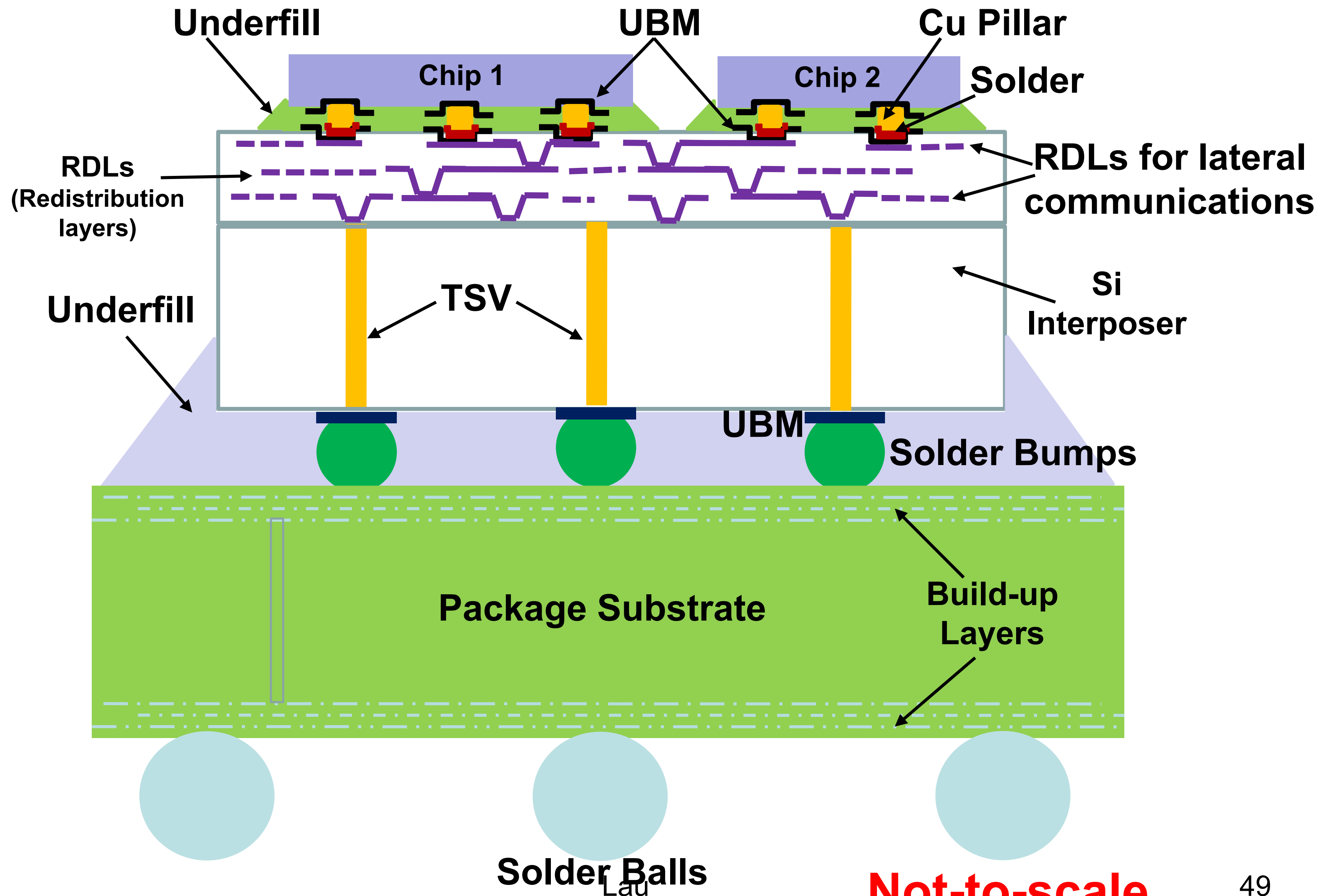
In general, a package substrate with 8-build-up-layer (4-2-4) and 25µm line-width and spacing is more than adequate to support most of the chips. Thus, interposers are not needed.

Also, in the past 3 years, Substrate Houses have been developing package substrates with high build-up layers (5-2-5) and fine (12-15µm) line-width and spacing with 90% yield (not samples).

For example, at IEEE/EPTC (December 2012) SEMCO told us that they can make package substrates with (6-2-6) and 10-12µm line-width and spacing with 90% yield.

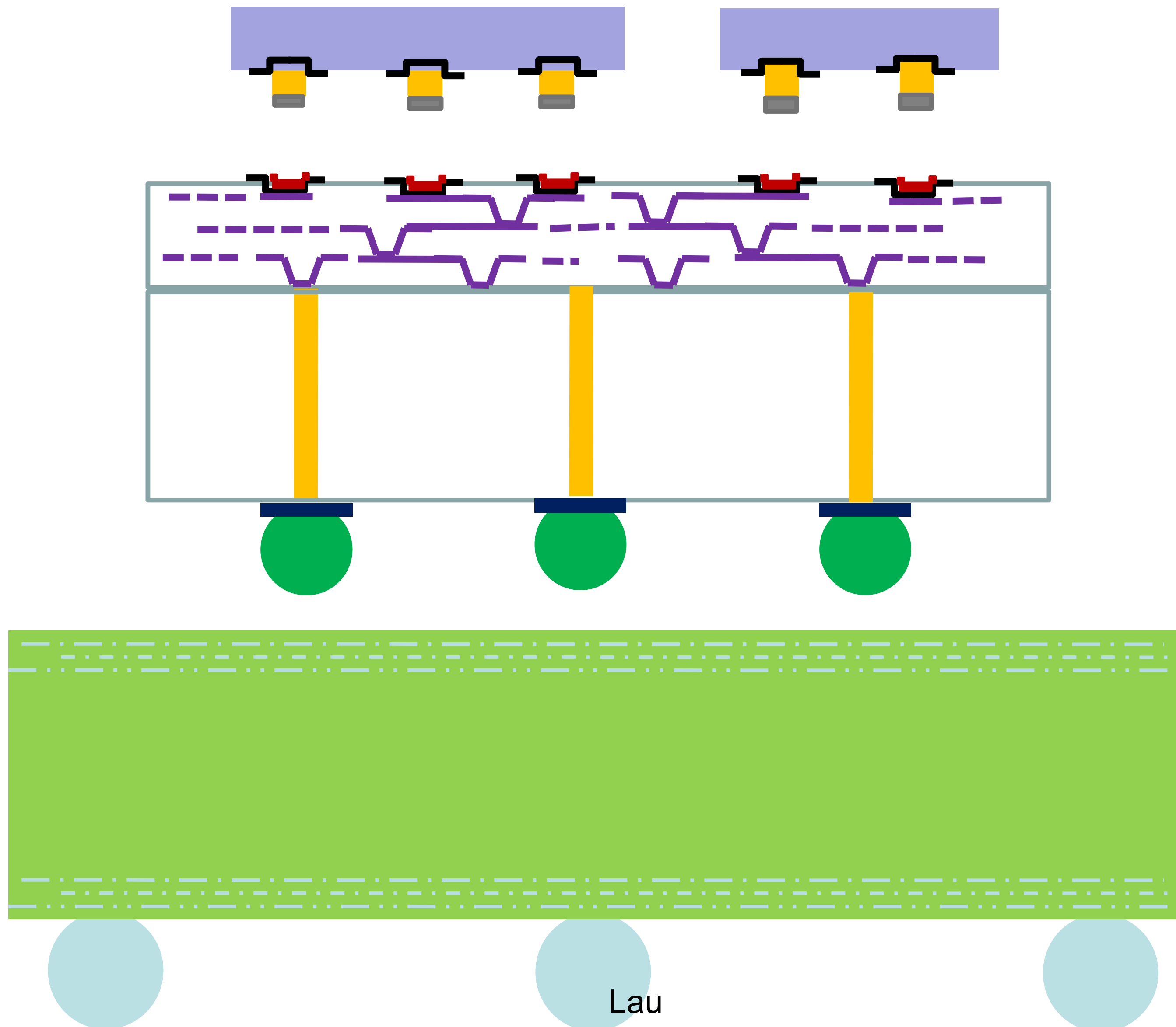
All these activities are keeping interposers away from volume production, except for very niche (such as extremely high-performance and high-density) applications.

Assembly of 2.5D IC Integration (Interposers)



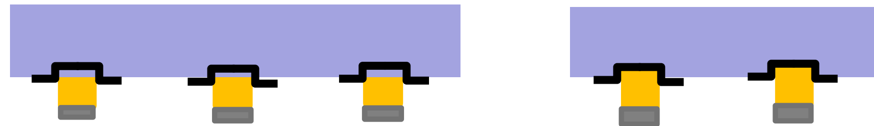
Not-to-scale

Fabrication of 2.5D IC Integration

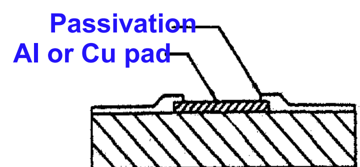


Fabrication of 2.5D IC Integration

Wafer Bumping
(Cu-Pillar with Solder Cap)

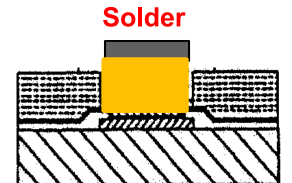


Cu Pillar with Solder Cap Wafer Bumping of the Device Chips

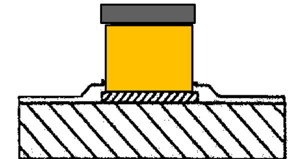


(1) Redefine Passivation

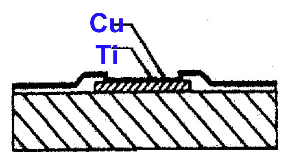
(3) Coat with Resist



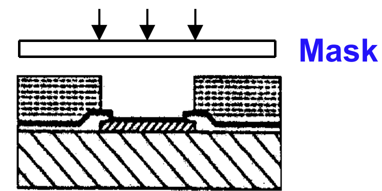
(5) EP Cu and solder



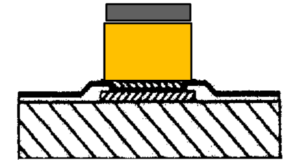
(7) Strip Cu/Ti



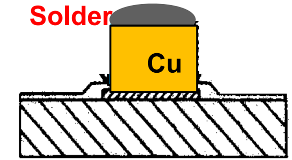
(2) Sputter Ti/Cu



(4) Pattern for the Cu-pillar



(6) Remove Resist



(8) Flux and Reflow

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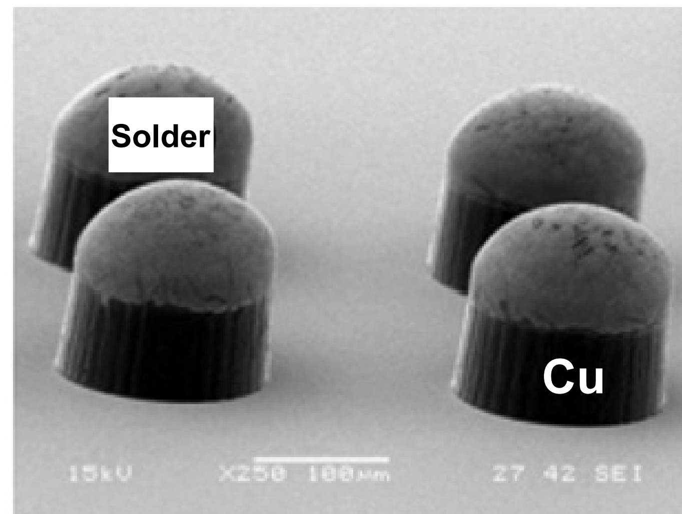
Cu Pillar with Solder Cap on the Device Chips



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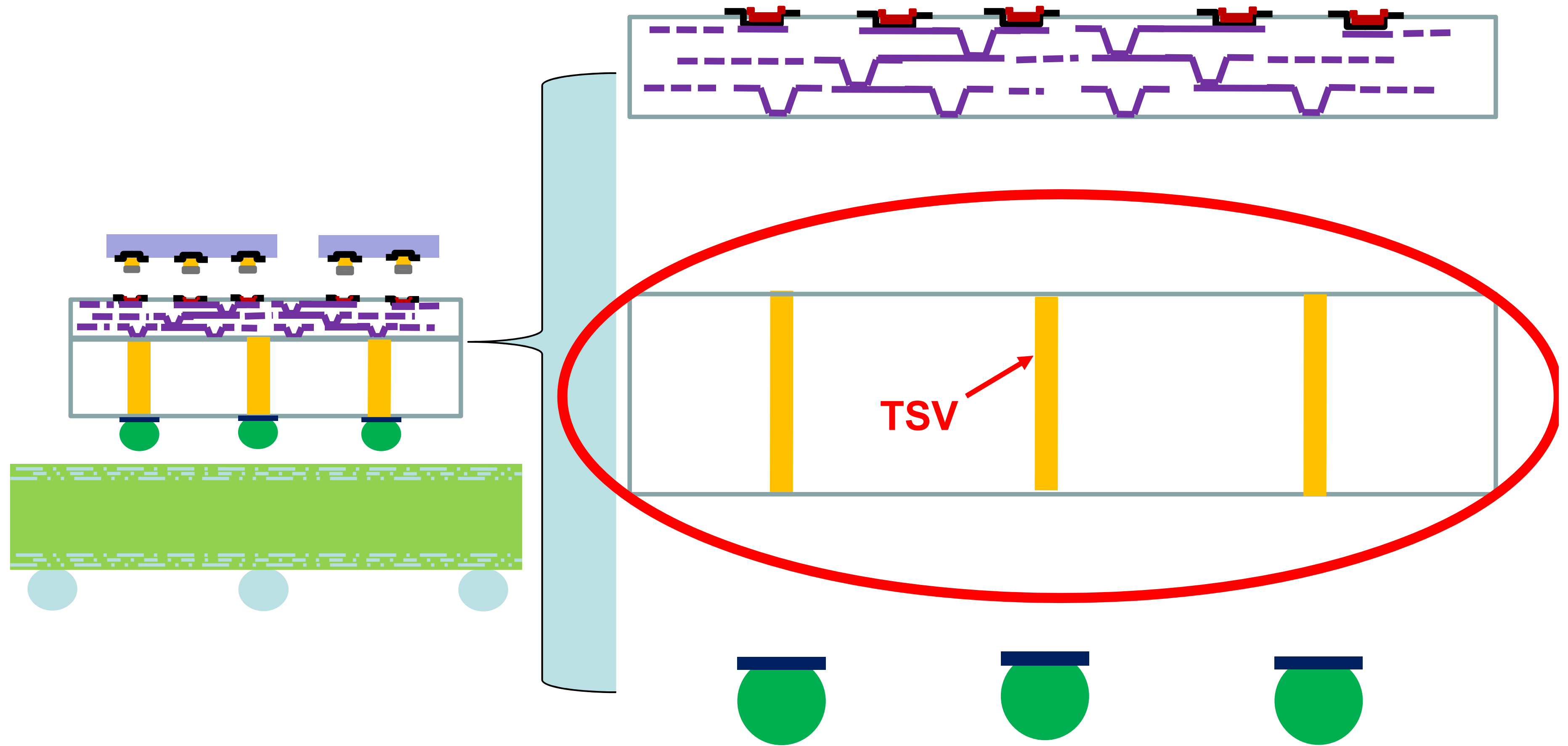
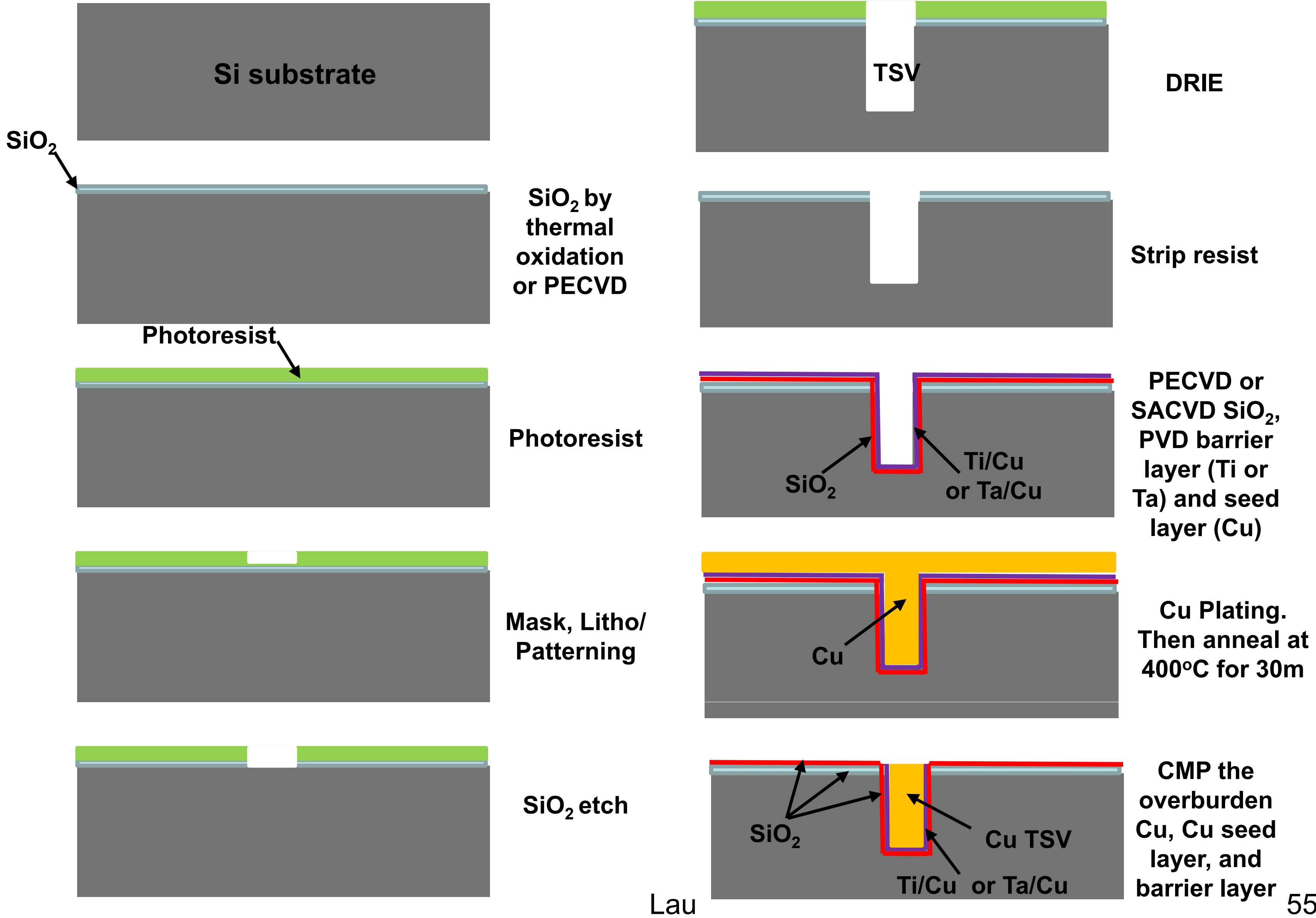
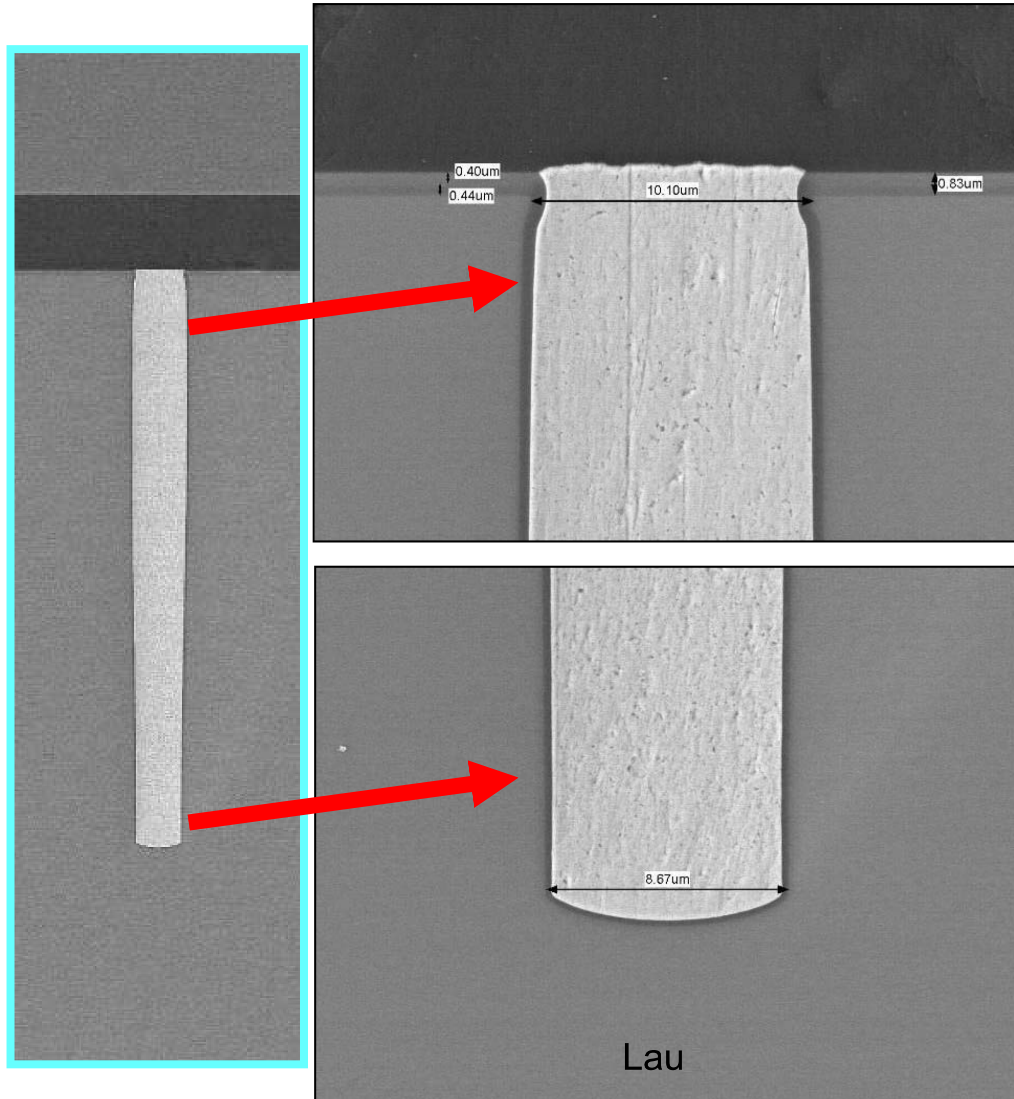
Fabrication of 2.5D IC Integration (TSV)



TSV Process Flow



Fabricated TSV



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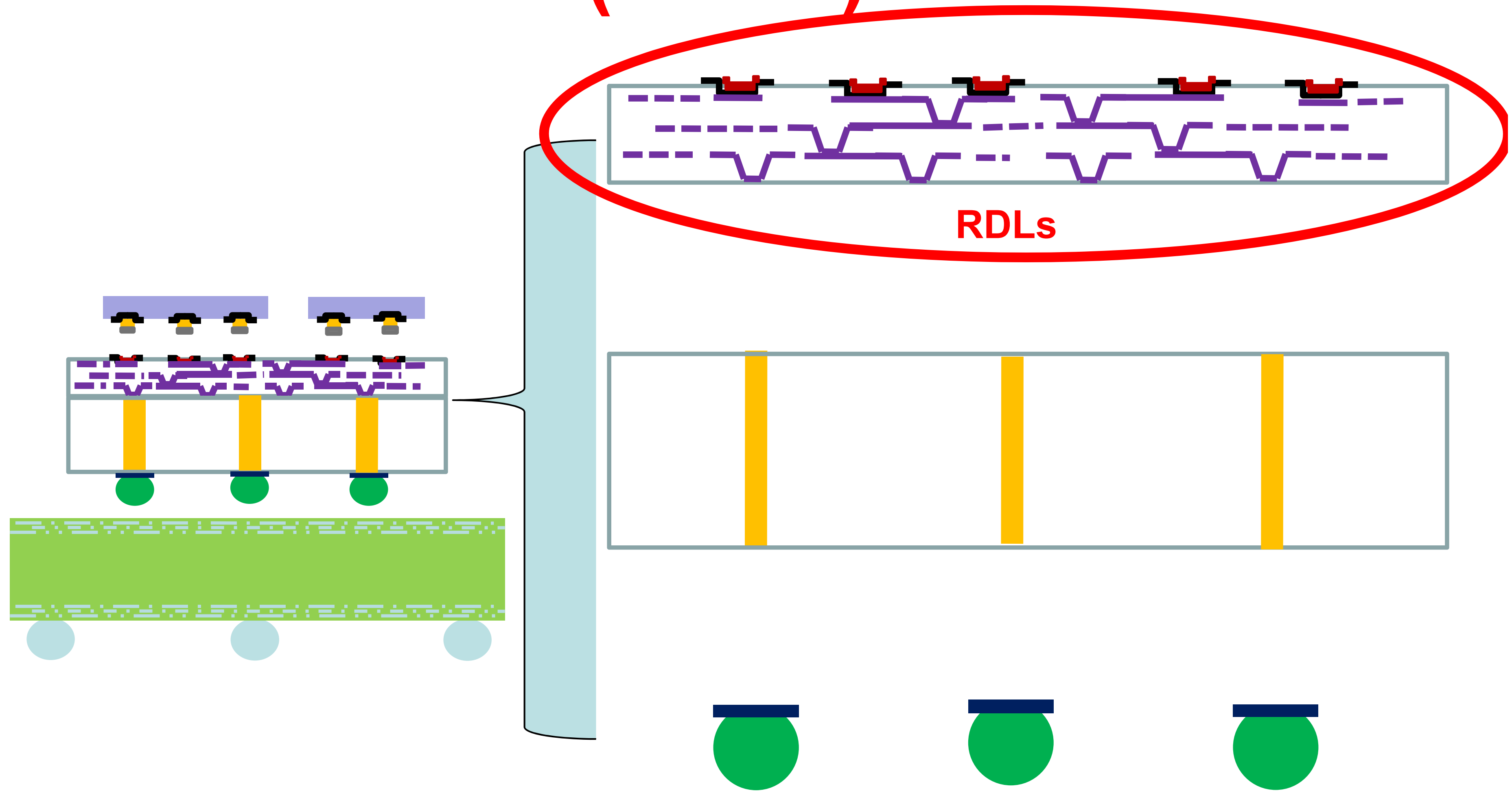
Fabrication of 2.5D IC Integration (RDLs)



Methods in Fabricating the RDLs in 3D IC Integration

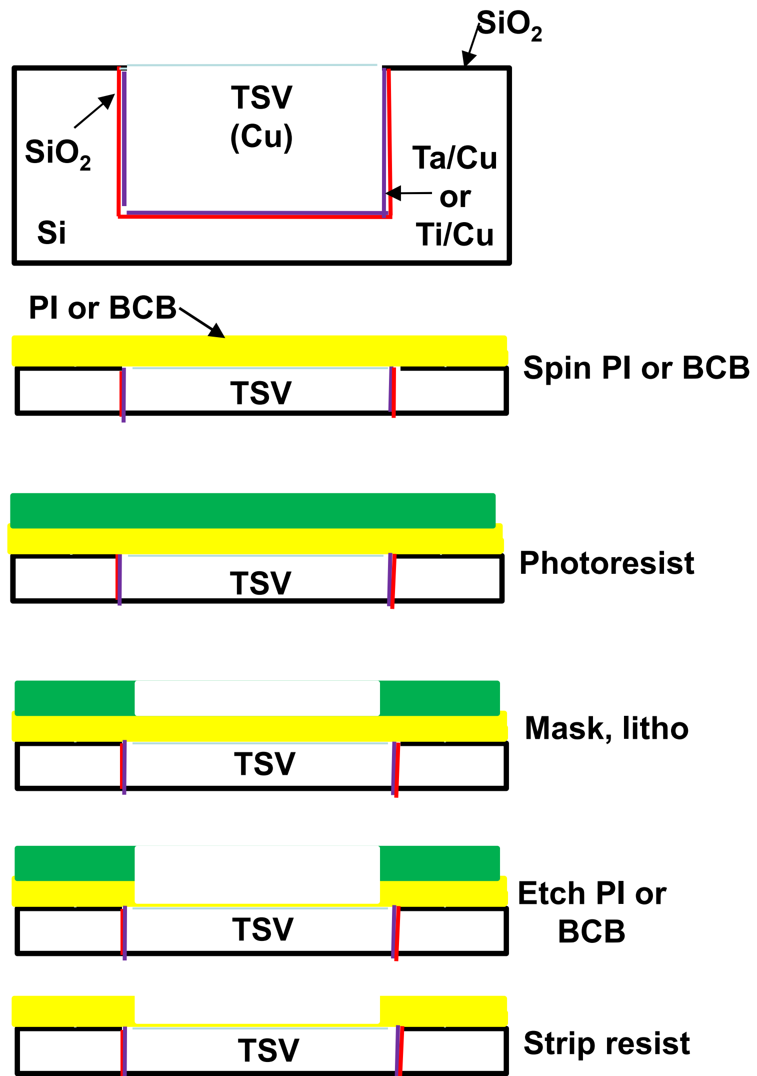
There are at least two ways to fabricate the RDL:

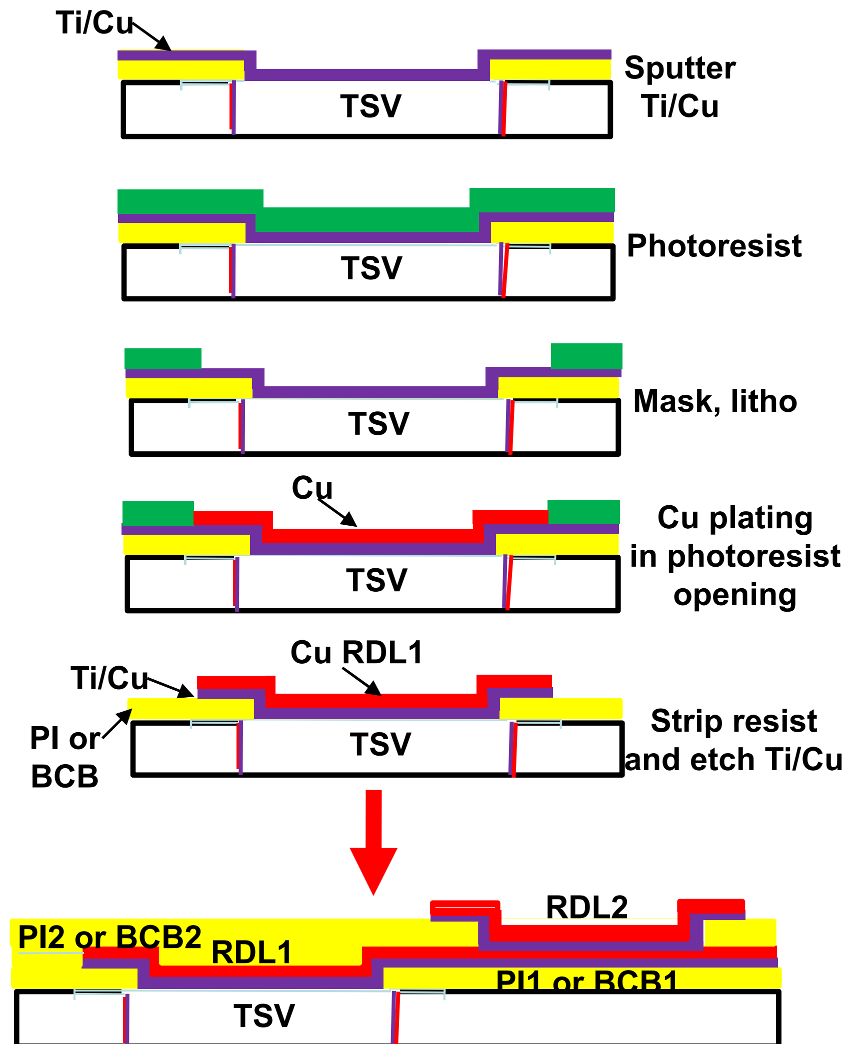
One is by using polymers such as polyimide (PI) or benzocyclobutene (BCB) to make the passivation layer and electroplating such as Cu to make the metal layer.

The other is by using the Cu damascene technique which is primarily modified from the conventional back-end-of-line to make the Cu metal layers.

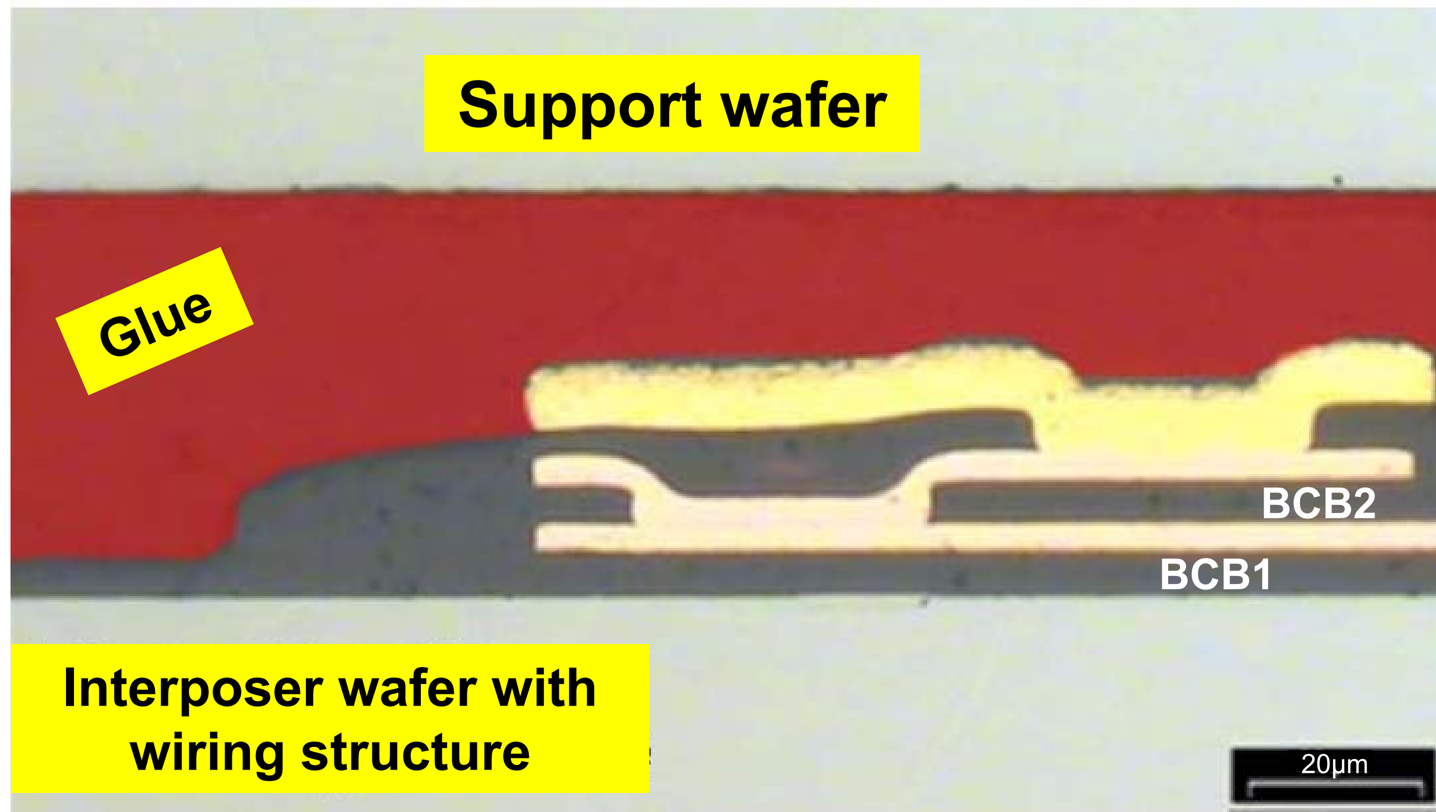
RDLs Fabricated by Polymer and Cu Plating

Fabrication of RDLs by Polymer





IZM's Fabricated RDLs with Polymer (BCB)



RDLs Fabricated by Cu Damascene

Process Flow for Fabricating RDLs by Cu Damascene

TSV (Cu)
SiO_2
SiO_2
Ta/Cu or Ti/Cu
Si

SiO_2
TSV — SiO_2 by PECVD

TSV — Photoresist

TSV — Mask, litho

TSV — RIE of SiO_2

TSV — Strip resist

TSV — Sputter Ti/Cu and plate Cu

V01 TSV — CMP Cu and Ti/Cu

TSV V01 — SiO_2 by PECVD

TSV V01 — Photoresist

TSV V01 — Mask. litho

TSV V01 — RIE of SiO_2

TSV V01 — Strip resist

TSV V01 — Sputter Ti/Cu and plate Cu

RDL1 TSV V01 — CMP Cu and Ti/Cu

RDL2
DL2
V12
DL12
DL1
RDL1
DL01
TSV V01

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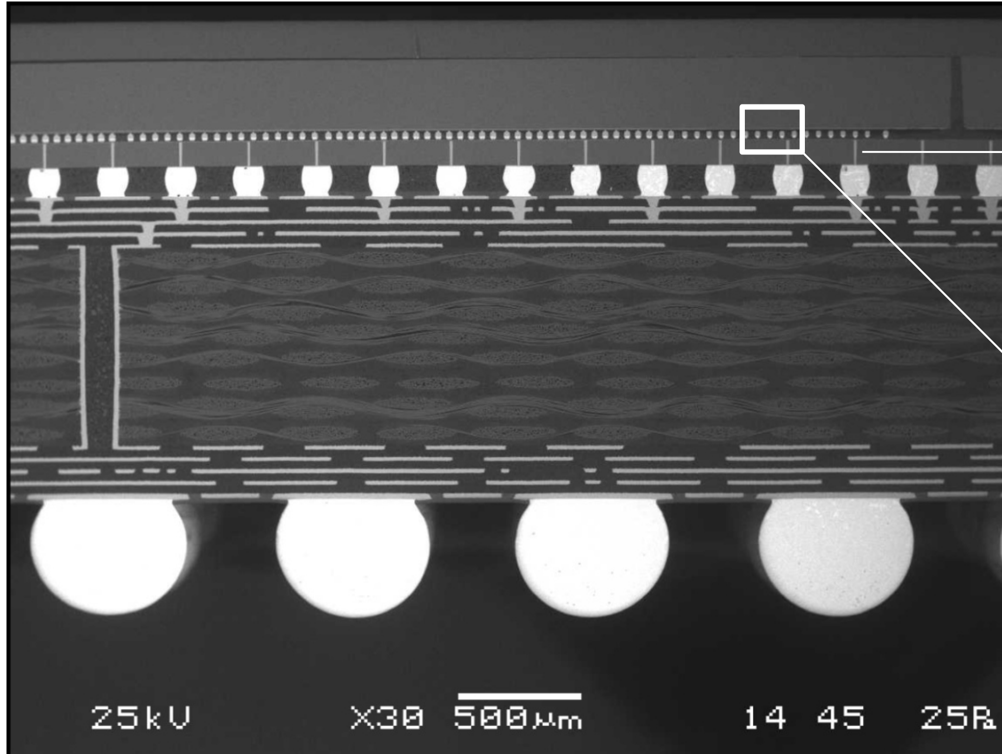
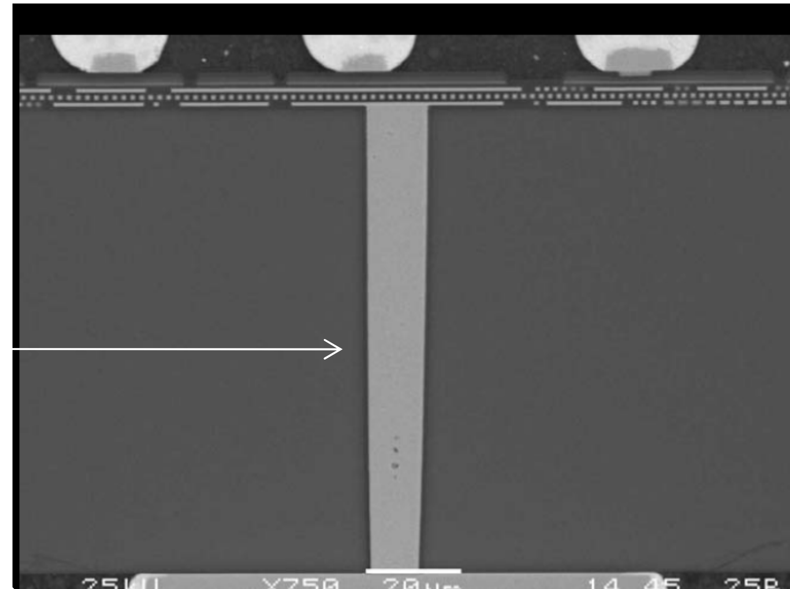
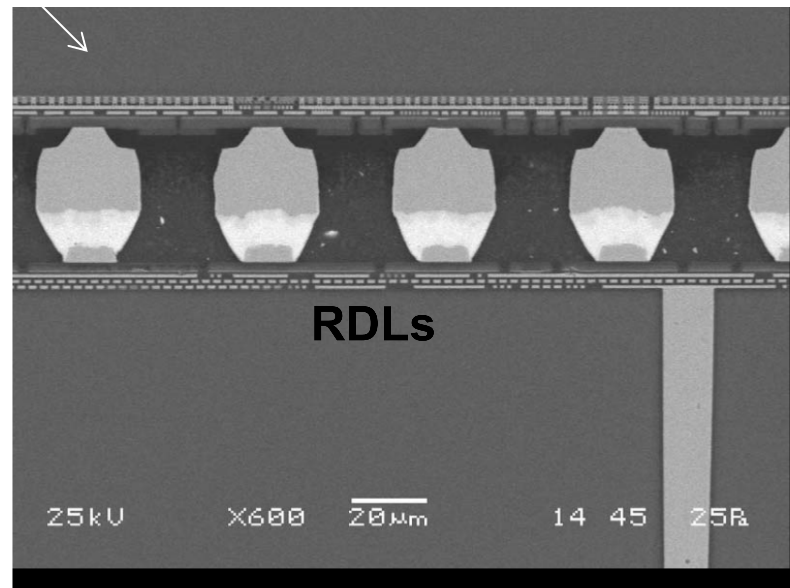
Xilinx/TSMC's FPGA Wide I/O Interface

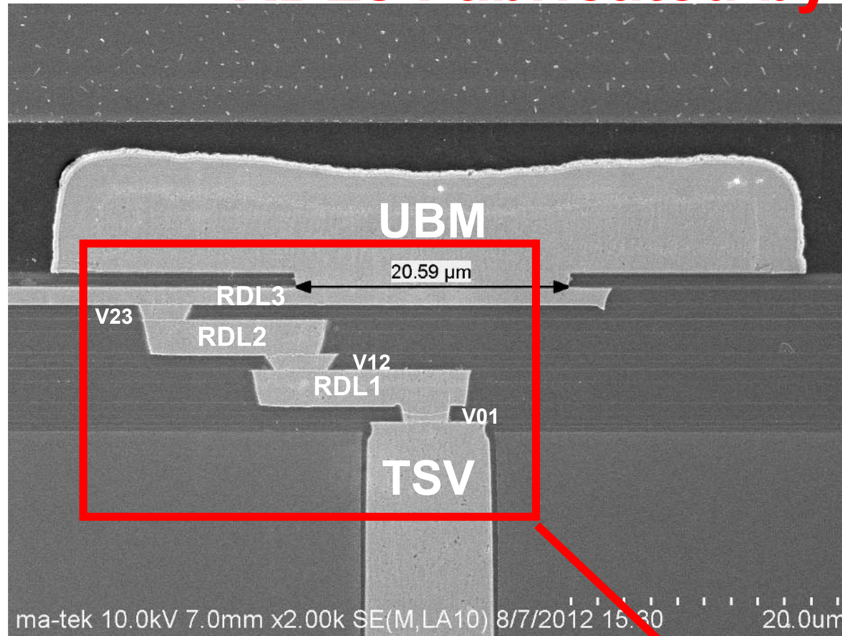


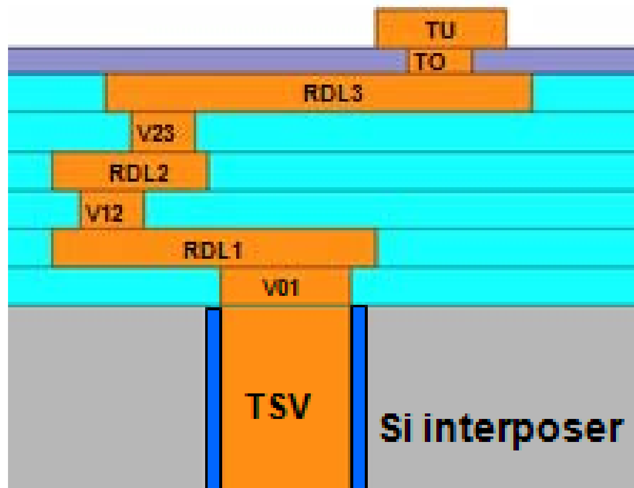


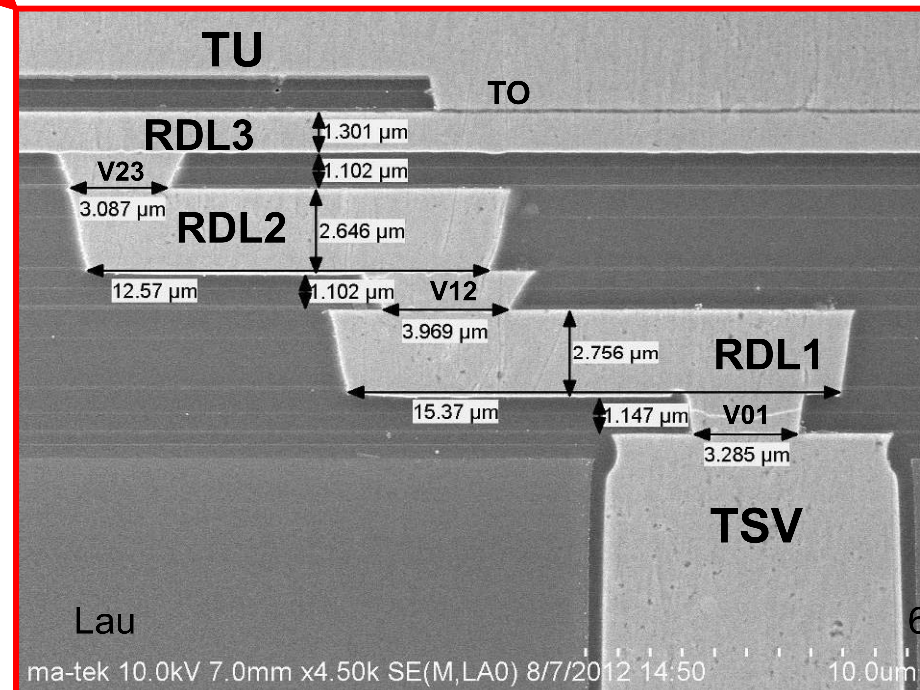


Xilinx/TSMC 2011 ECTC

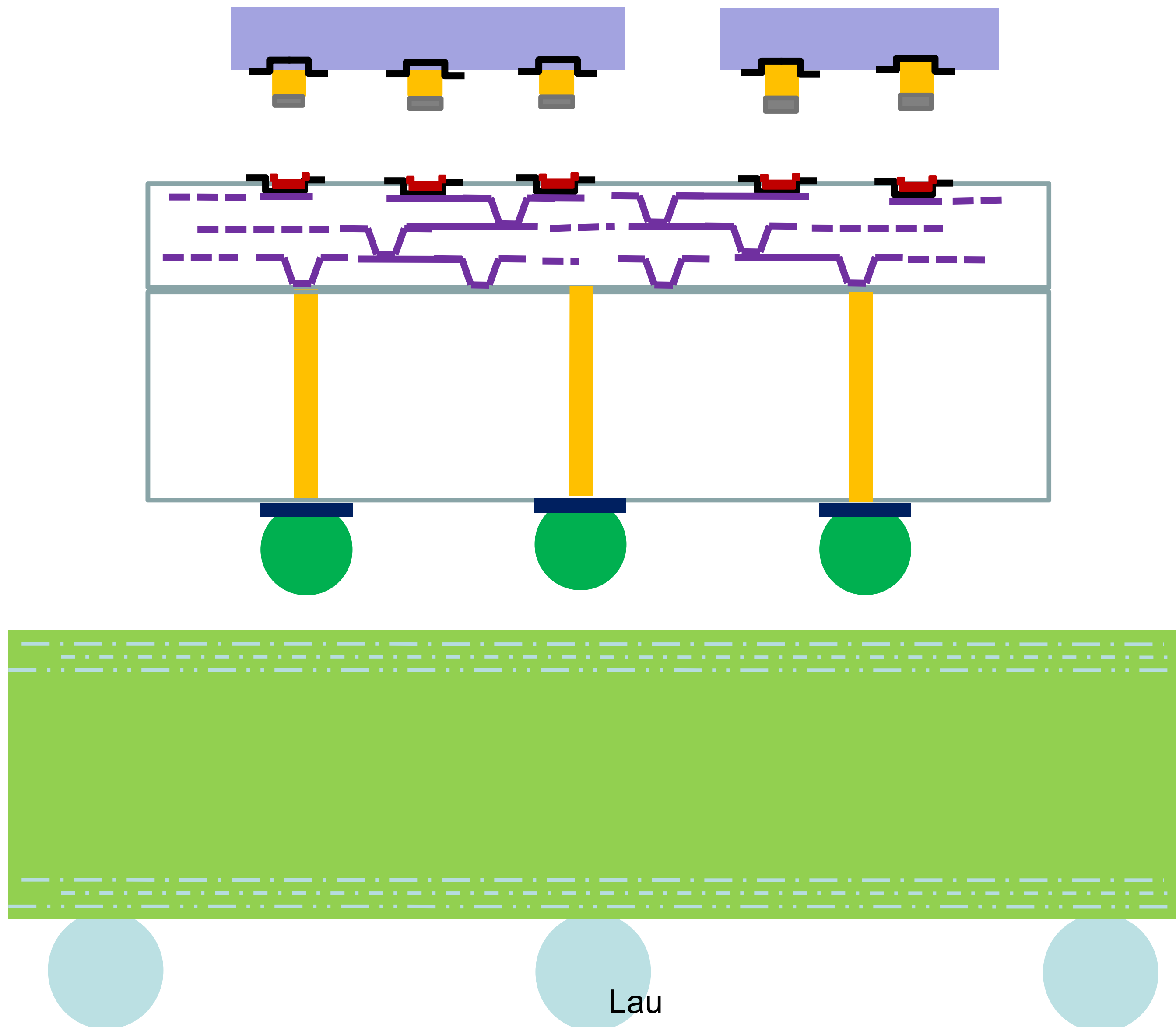
RDLs Fabricated by Cu Damascene







Fabrication of 2.5D IC Integration



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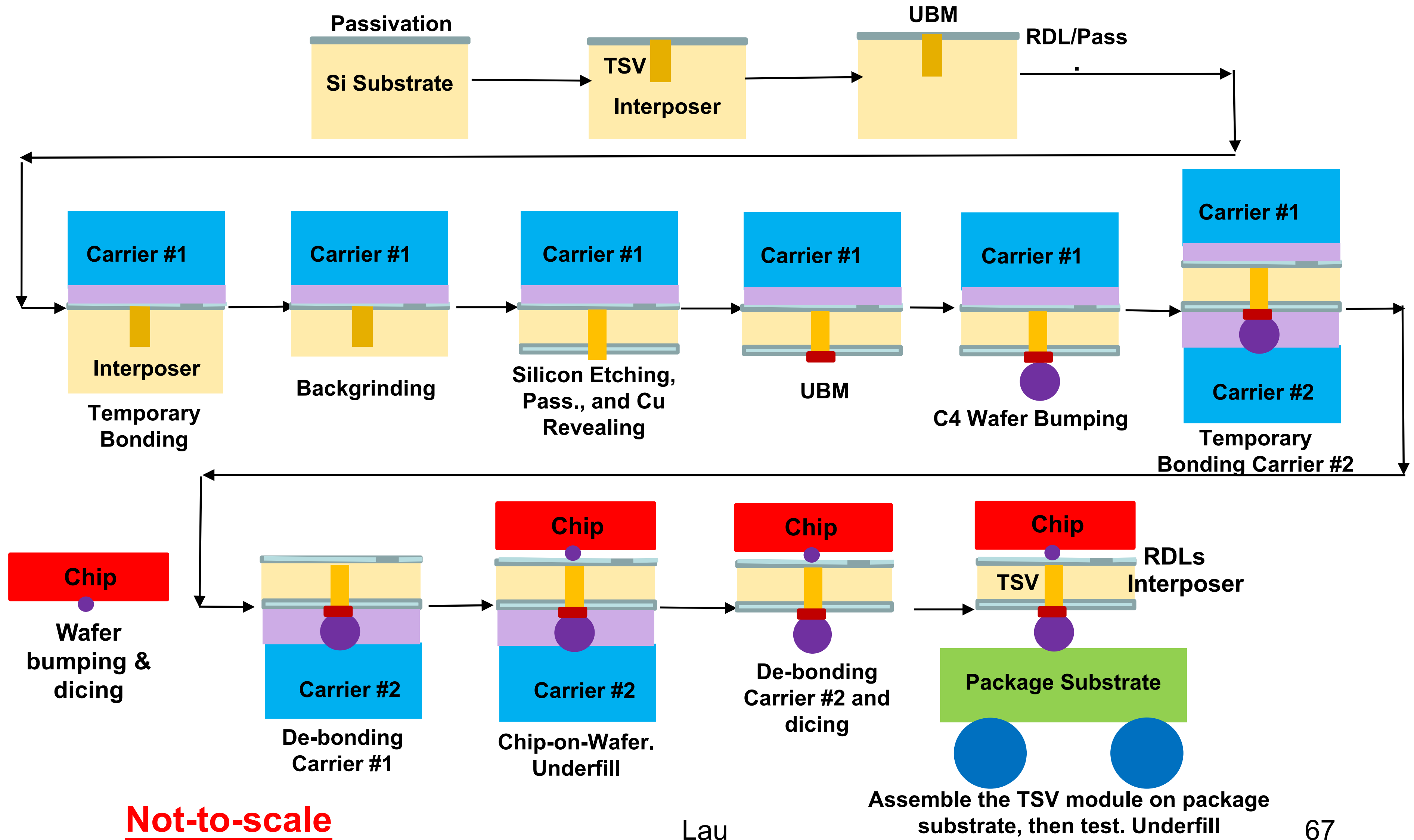
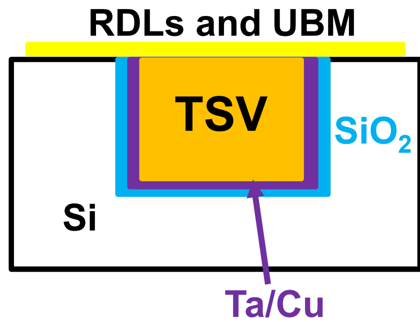
Conventional Process Flow of 2.5D IC Integration

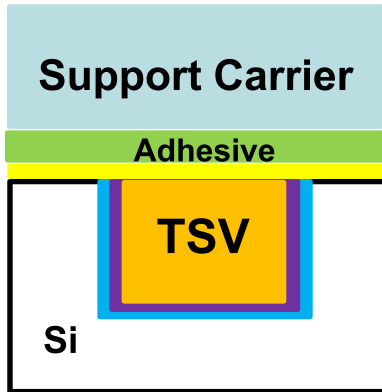


Not-to-scale

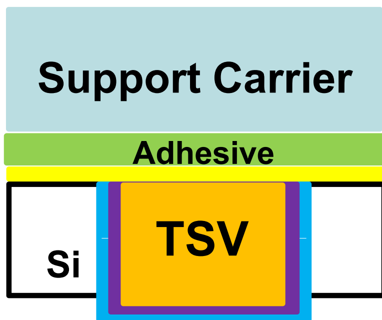
TSV Cu Revealing



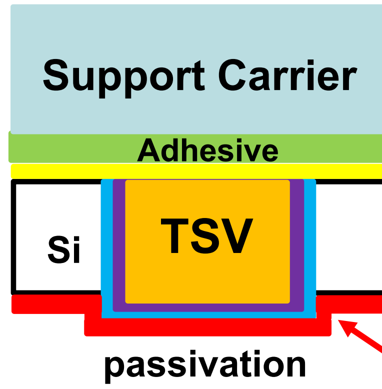
Complete frontside RDLs & UBM



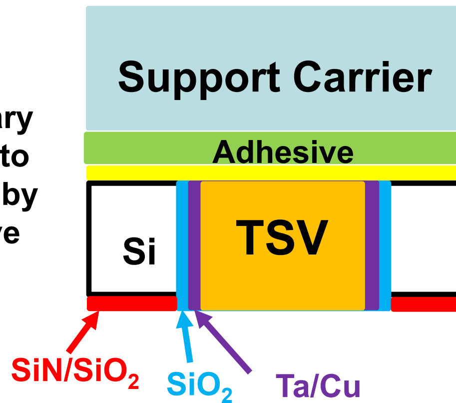
Temporary bonded to a carrier by adhesive



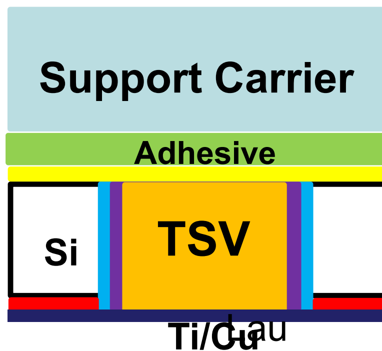
Si dry etch (RIE)



Low temperature SiN/SiO$_2$



CMP for SiN/SiO$_2$ buffing, and barrier and Cu polishing



Sputter Ti/Cu

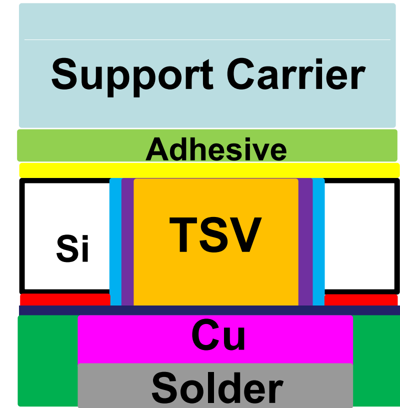
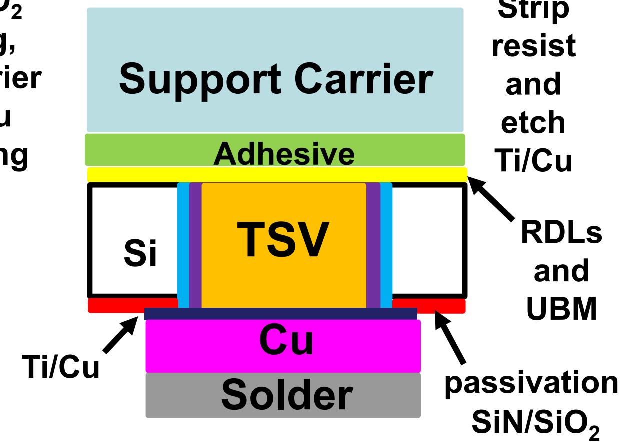


Photo-resist, Mask, litho, Cu plating, solder plating

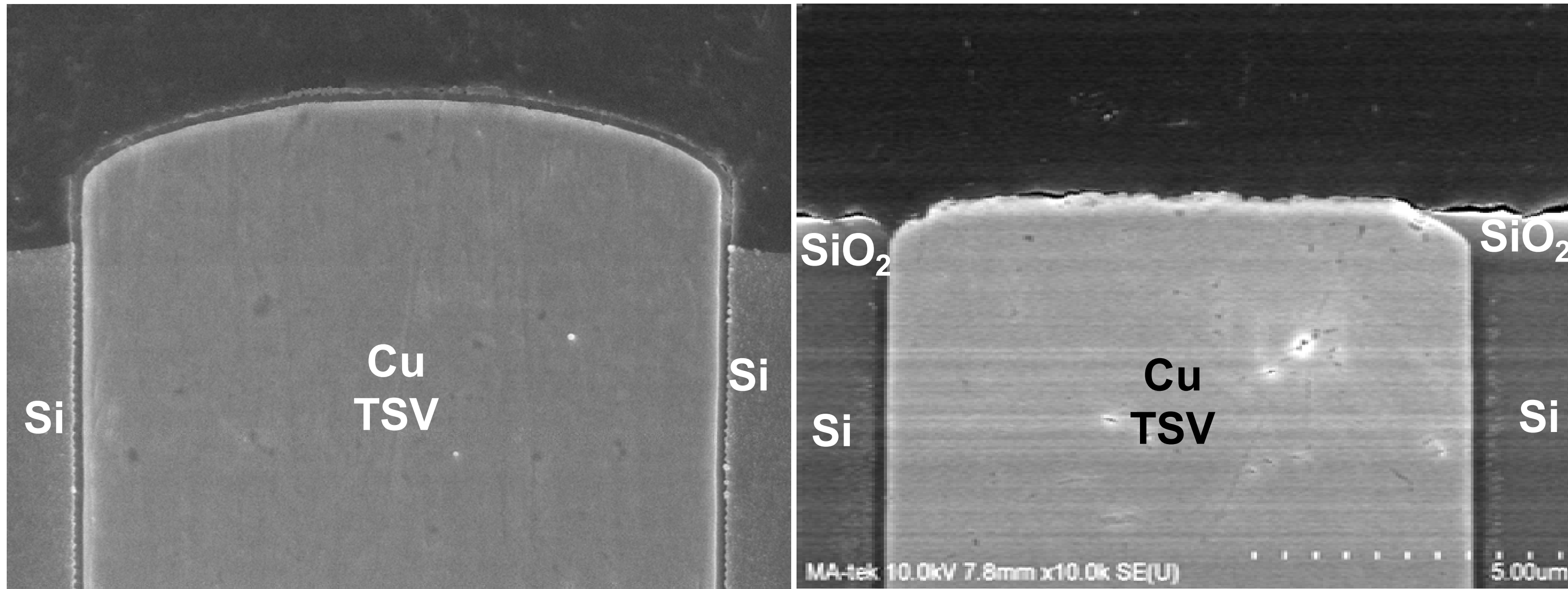


Strip resist and etch Ti/Cu

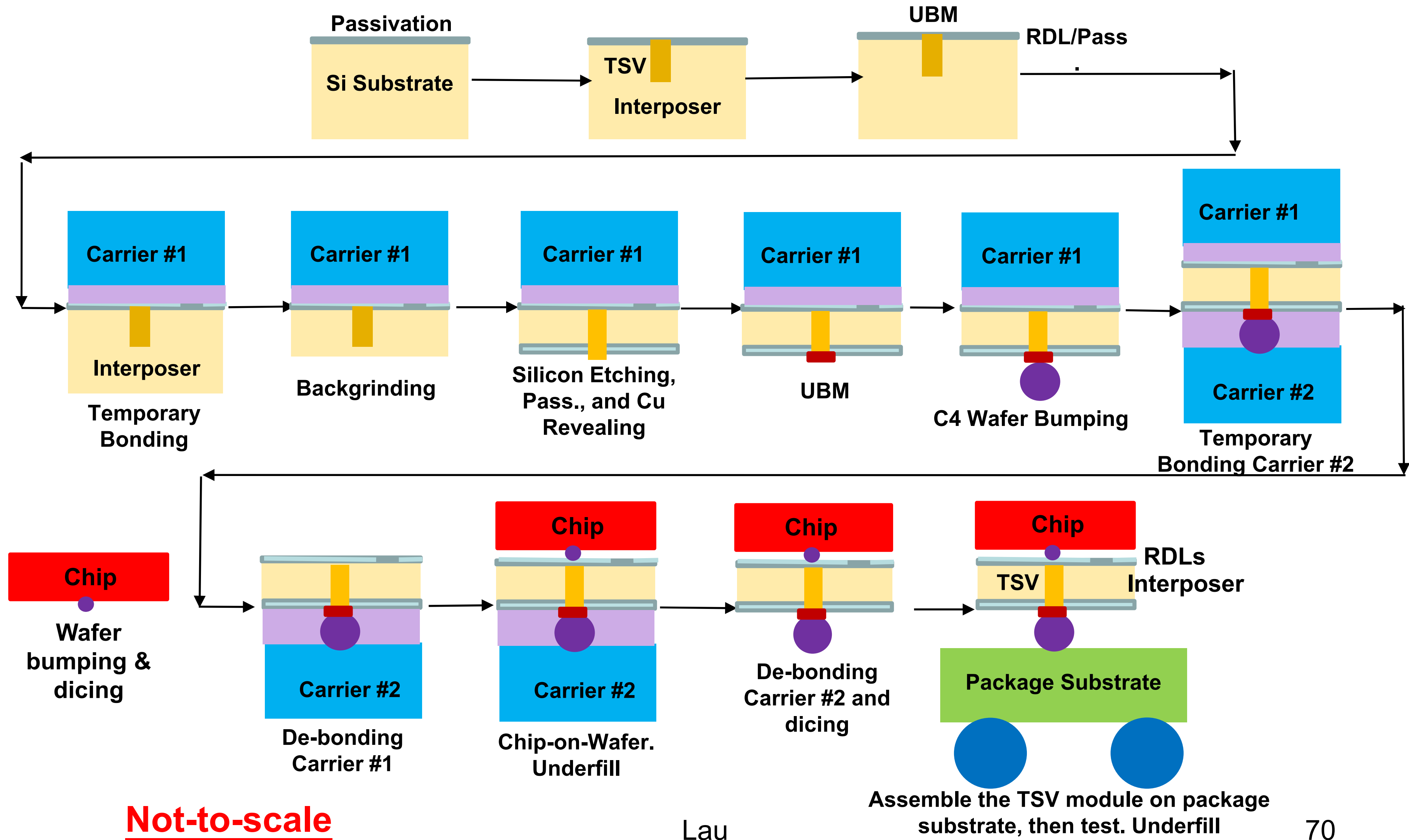
Not-to-Scale

Lau

TSV Cu revealing. (Left) Before dry etch of Si. (Right) After Si dry etching, low-temperature SiN/SiO_2, and removal (CMP) of the isolation layer

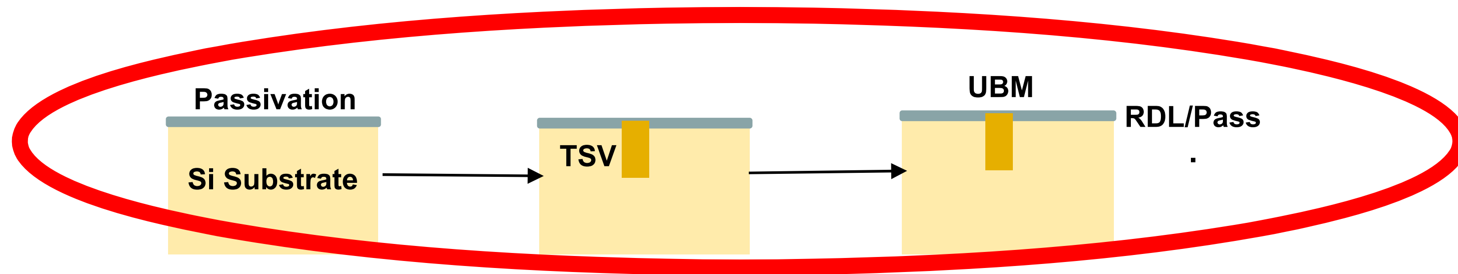


Conventional Process Flow of 2.5D IC Integration



Not-to-scale

Conventional Process Flow of 2.5D IC Integration



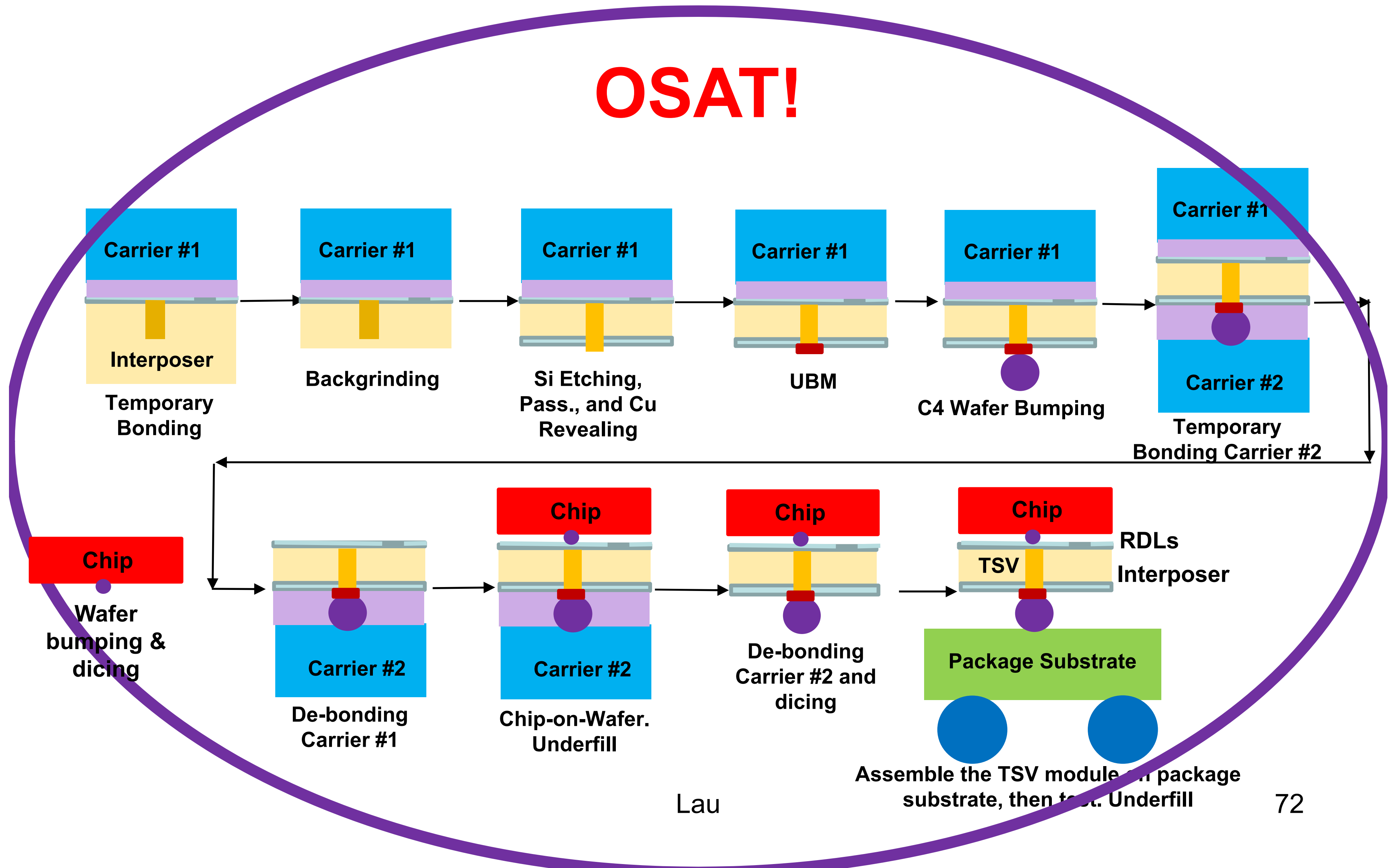
FABs who made the high-performance chips which needed the support of an interposer

and

Interposer Foundries!

Conventional Process Flow of 2.5D IC Integration

(Except vertically integrate companies, e.g., TSMC and Samsung)



Who Does the MEOL?

For the thicknesses of memory-chip stacking and DRAMs in HMC, and active and passive interposers, all the TSVs fabricated are blind vias.

The blind TSV wafer is followed by solder bumping / temporary bonding / backgrinding / TSV revealing / thin wafer handling / de-bonding / cleaning, which are called MEOL (Middle-end-of-line).

Except the vertically integrated companies, e.g., TSMC and Samsung, the MEOL is better to be performed by the OSAT.

Supply Chains for 2.5D IC Integration

1. For passive interposer wafers, the TSV can be done by either the FAB or OSAT. For ≥3μm line width and spacing RDLs, FAB and OSAT can do it. Otherwise, it should be done by the FAB. However, for most interposers, the line width and spacing are in submicron, then most likely, the FAB or Interposer Foundries will do it.

2. For TSV passive interposer wafers, the MEOL, assembly and test should be done by the OSAT (except vertically integrated companies). There are many important tasks in the MEOL (solder bumping / temporary bonding / backgrinding / TSV Cu revealing / thin wafer handling / de-bonding / cleaning), assembly and test; thus the OSAT should strive to make themselves ready for a robust and high yield manufacturing process.

3. In order to avoid finger pointing and have a smooth hand-off from the FAB to OSAT of the un-finished (blind) TSV wafers, more research and development works should be performed on the testing methods of the blind TSV wafers for electrical, thermal, and mechanical performances.

Summary and Wishful Thinking

- A few years from now, when 2.5D and 3D IC integrations are in volume production, people will mention CIS and MEMS with TSVs less.

- For device wafers, TSVs straight through the same memory chips to lower the power consumption, increase the bandwidth, and reduce the form factor is the right way to go and will be the major applications of 3D IC Integration!
  - For memory-chip stacking, hopefully, Samsung/Hynix will start shipping small volume in 2015 and ramping up the production in 2016.
  - For wide I/O DRAM (Hybrid Memory Cube), hopefully, according to the SPEC, Micron/IBM and Samsung come out with some samples this year, take some order for samples in 2014, small volume production in 2015, and ramp up the production in 2016.

- For device-less wafers (passive interposers):
  - When TSVs are used for very high-performance and high-density (niche) applications, hopefully, TSMC will help Xilinx and Altera to ship samples to their potential customers in 2014, small volume production in 2015, and ramp up the production in 2016. Also, Globalfoundries and UMC will ship small volume of interposers in 2015.
  - When TSVs are used for niche (e.g., military) products, hopefully, Interposer Foundries are ready.

- OSAT should strive to make themselves ready for a robust and high yield MEOL, assembly, and test manufacturing process.

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Thank you very much for your attention!

Lau